Integration, the VLSI Journal xxx (2017) 1–18

Contents lists available at ScienceDirect

Integration, the VLSI Journal

journal homepage: www.elsevier.com/locate/vlsi

Offline Testing of Reversible Logic Circuits: An Analysis

Hari Mohan Gaur [a,*], Ashutosh Kumar Singh [b], Umesh Ghanekar [a]

[a] Department of ECE, NIT Kurukshetra, Haryana, India
[b] Department of Computer Applications, NIT Kurukshetra, Haryana, India

ARTICLE INFO

Keywords:
Reversible logic
Offline testing
Fault models
Performance parameters
ATPG
DFT

ABSTRACT

Reversible logic is one of the foregrounds to meet the ever-changing demands electronic devices with its applications to quantum computation. The change in technology gives rise to new challenges; consequently numerous fault model came into the existence where testing plays a significant role to achieve desired results. Several testing methodologies have been proposed for the identification of different types of fault models in reversible logic circuits and are scaled on various performance parameters. We bring collective information of fault models, performance parameters and offline testing approaches from the literature where aim is to obtain a near optimal solution by efficiently exploring the entire space. The paper critically analyses a range of testing strategies reported by the researchers and presented in two broad classifications, namely automatic test pattern generation (ATPG) and design for testability (DFT) methodologies. All the methods are explained in detail with a brief illustration. Comparison results are presented in tabular form highlighting preeminent among all methodologies on the basis of performance parameters.

1. Introduction

Smaller transistors will no longer results faster and efficient and further miniaturization does not seem to be promising way in the development of compact electronic devices due to the breakdown of Dennard scaling [1]. Reversible logic is one of the alternative techniques to meet the demand of low power, high speed compact devices with its applications most emerging technologies including to quantum computation, DNA computation, optical computation etc. It guarantees nearly energy free computation by preventing power dissipation in form of information loss as in irreversible operations [2,3]. The researchers are at par with the latest innovations in this area to develop designs of several logical and benchmarking circuits on the top of various synthesis algorithms [4–8]. These circuits are based on distinguished gate libraries and their efficiency is governed by their operating costs [9]. Researchers are also showing their remarkable efforts of design of several reversible circuits using quantum-cellular automata [10,11], optical computing and traditional technologies [12–17] for the successful establishment of reversible logic.

Testing of irreversible circuits has been extensively studied in 70s, however, reversible logic has been limited studied by researchers and there is a lot more to be done to achieve desired results. Testing guarantees the true functioning of electronic devices which shows its untamed necessity for their perfection. Offline and online testing are the two approaches of detecting faults in any system and in reversible logic as well. A circuit is said to be online testable if it is able to find fault within the circuit during its operation and in case of offline testing, a number of test vectors are applied after taking out the circuit from its usual operation for which correct output values are known. We are concerned here for offline testing approaches as it is gaining ground over online testing since the later approach entails a large increase in quantum cost which probably increases the power dissipation. All the existing reversible logic testing approaches that have been proposed previously are divided into these two major categories for the detection of a new family of fault models. Further classification is given on the basis of different methodologies of testing the reversible logic circuits, deterministic and randomized automatic test pattern generation (ATPG) [18–28] and design for test methodology (DFT) [29–33] in case of offline testing. Designing with novel gates [34,35], designing with existing circuit [36–38] and designing with inbuilt testability [39] can be found in case of online testing [40,41] as shown in Fig. 1. The efficiency of these methodologies is governed by several performance parameters. The metrics for ATPG methodologies include test size, execution time and fault coverage and efficiency of DFT methodologies are directed by increase in quantum cost, gate count and number of inputs including the previous three. The execution in terms of decrease in test size and percentage increase in

* Corresponding author.
E-mail addresses: leoharimohan84@gmail.com (H.M. Gaur), ashutosh@nitkkr.ac.in (A.K. Singh), ugnitk@nitkkr.ac.in (U. Ghanekar).

https://doi.org/10.1016/j.vlsi.2018.01.004
Received 10 November 2016; Received in revised form 18 November 2017; Accepted 8 January 2018
Available online xxxx
0167-9260/

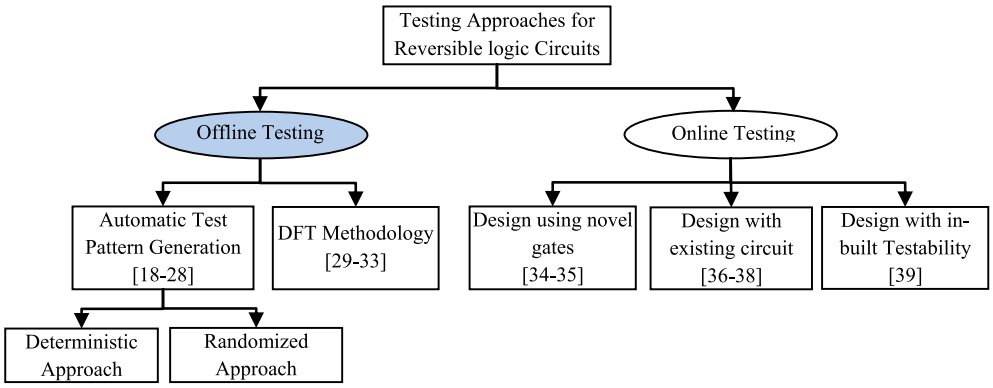

Fig. 1. Classification of testing approaches.

quantum cost has improved over the years but for some type of fault models. Argument and debates are still remaining for obtaining best suitable algorithm which derives minimum complete test set which cover all fault models in minimum execution time. Since, different type of fault model has different significance and has different method of detection in reversible circuits.

Moreover, reversible logic performs bijective functions where a unique output state is obtained from every input state. The number of inputs is same as number of outputs that produce fully controllable and observable operations. The logic values at each node can be applied and can be detected at the output for taking test judgments, which in turn makes testing easier than that for irreversible logic circuits. Also, some challenges have arisen as a consequence of new technology in view of performance parameters. Some major challenges pertaining offline testability includes:

- ➢ Design complexity due to high density of gates in reversible circuits.
- ➢ Test data minimization as there are 2^n configurations to be executed, which is very large for bigger circuits and requires more execution time.
- ➢ Very low signal levels as compare to that of irreversible logic circuits.
- ➢ A variety of new fault models that have their unique detection procedure which should be covered in minimum data set.
- ➢ Fanout and Feedback, a technology problem which is not permitted in reversible circuits.

The rest of the paper is structured as: First, the preliminaries associated with offline testing, which include basics of reversible logic, fault models, performance parameters and notations are summarized in section 2. Second, various testing methodologies from the literature are explained in detail by differentiating them into subsequent categories. These methodologies are summarized and compared in a table based on their format, highlighting the optimum among them in section 3, section 4 and section 5. The combined performance analysis of all the approaches based on performance parameters on available circuits referred by the authors, with considered fault models and is given section 6 followed by conclusion and future scope in section 7.

2. Preliminaries

2.1. Reversible logic gates and libraries

A logic function with n Boolean variables is a *reversible function* if it maps distinct input to distinct output, i.e. there should be $n \times n$ bijective function mapping between input and output. A *reversible gate* realizes a reversible function. If a k input k output gate that produce distinct output for its distinct input functions is called as $k \times k$ reversible gate. Various reversible gates are given in literature. Some of the standard gates are NOT, CNOT, Toffoli, Fredkin and Peres gates [41].

Any of a reversible circuit can be synthesized using these basic gates and their extended versions. This tends to the formation of gate libraries. A *reversible gate library* defines a set of basic reversible gates which can be used to synthesize a reversible circuit using different algorithms. Multiple controlled Toffoli (MCT) or k-CNOT, multiple controlled Fredkin (MCF) and NOT-CNOT-Toffoli (NCT) are widely used reversible gate libraries [41]. These libraries can be used alone or in the combination of two or more, depending on the algorithm.

2.2. Fault models

Faults are any kind of imperfection in a circuit which affects the functional behaviour of a system permanently or for a finite interval of time due to any manual and environmental issues [41]. These are called as permanent and non-permanent types of faults respectively. The offline approach finds its application to detect only permanent faults whereas online approach is more suitable for non-permanent type of faults. In this review paper, we focused only on permanent faults which permanently transform the operation of the circuit. A fault model describes the type of fault occurred in a circuit and identifies the target of testing. There are several fault models and their types are proposed in the literature. In the correspondence, we focus only on structural fault models in reversible logic circuit shown in Fig. 2.

Following is the brief definition of fault models depicted in Fig. 2 from left to right.

2.2.1. Stuck-at fault

Like traditional stuck-at fault model, this type of fault occurred in a circuit when any wire fixed on a single value 0 or 1, called as stuck-at 0 or stuck-at 1 fault respectively.

2.2.2. Bridging fault

Similar to traditional fault model, this type of fault takes place when two adjacent lines in a circuit get physically bridged or shorted by means of wired AND/OR interconnections as a result the response comes an erroneous value.

2.2.3. Missing gate fault

A single missing gate fault is defined as complete disappearance of a reversible gate from a circuit and if two or more consecutive gates are disappeared then it is called as a multiple missing gate fault. Missing gate faults may also occur as *repeated gate fault* when any gate replicates its functionality in certain instances in a reversible circuit. If the number of instances are even, it affect in similar manner as of single missing gate fault and if the instances are odd in number then there will be no change in the functionality of the circuit. And as *partial missing gate fault* which occur when any control point loses its control from a gate in a reversible.