



Exploratory design of on-chip power delivery for 14, 10, and 7 nm and beyond FinFET ICs[☆]

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ABSTRACT

An exploratory modeling methodology is presented for estimating power noise in advanced technology nodes. The models are evaluated for 14, 10, and 7 nm FinFET technologies to assess the impact on performance. The power noise is composed of three parts, noise related to the global power grids, via stacks, and local power rails, based on the hierarchical nature of power distribution networks. In 14 nm technology, the global power noise dominates the total power noise. The power noise is lower and more evenly distributed in 10 nm technology. 7 nm technology is shown to be more sensitive to local power noise. To decrease the global power noise, extra metal layers are added to the global power grid. A 75% reduction in global power noise is observed in 14 nm technology. Stripes between local track rails are evaluated to reduce the local power noise, exhibiting up to 57% improvement in local power noise at the 7 nm technology node. As a promising alternative material for power network interconnects, few layer graphene is shown to exhibit good potential for reducing local power noise. The effects of different scaling scenarios of the local power rails on power noise are also discussed.

1. Introduction

The increasing demand for high density, high performance integrated circuits leads to aggressive technology scaling, enabling billions of transistors [1]. Due to the area and leakage current advantages as compared to planar CMOS, FinFETs have become the standard CMOS structure as technology is scaled below the 22 nm technology node [2]. While significant research effort is focused on deeply scaled transistors and emerging technologies, the RC interconnect impedance is challenging performance improvements brought by technology scaling. The parasitic capacitance of the local metal lines is less due to the adoption of low-k dielectrics and air gap interconnects [3]. The significantly increasing resistance of the local interconnects has however become the dominant limitation to performance improvements despite faster devices and greater levels of integration [4]. Scaling the cross sectional area of the local interconnects however quadratically increases the resistance. The resistivity of copper, used in traditional on-chip interconnects, sharply increases as the metal line pitch decreases [5], as illustrated in Fig. 1. In this case, the local power network is also highly resistive, leading to significant on-chip power noise.

Replacing copper interconnect with lower resistivity material interconnect is one way to reduce the effects of the “resistivity wall.” Silver is one of these materials whose bulk level resistivity is lower than copper. Due to the excellent conductivity of both heat and electricity, and the negative temperature coefficient of carbon-based material graphene, few layer graphene (FLG) and graphene nanoribbons (GNRs) have been considered as an alternative material for on-chip interconnects [6,7]. Graphene material has been listed in the technology roadmap from ITRS 2015 [4] and many industrial research centers [8]. The thin film resistivity of three materials, silver, FLG, and GNRs, has been investigated, respectively, in [9–11]. A comparison of the resistivity of different materials with interconnect width scaling is also illustrated in Fig. 1. The thin film resistivity of silver increases significantly at 50 nm, and eventually becomes larger than copper as the metal line pitch is scaled to 10 nm. By intercalating FLG with ferric chloride, a sheet resistance of $8.8\Omega/\square$ has been reported [11]. Based on the thickness of five layer graphene, the resistivity of FLG is lower than copper, particularly when the metal line pitch is small, making FLG a promising material for a highly resistive local power network. GNR exhibits a higher resistivity comparable to copper when the metal line pitch is small (from 40 nm to 10 nm).

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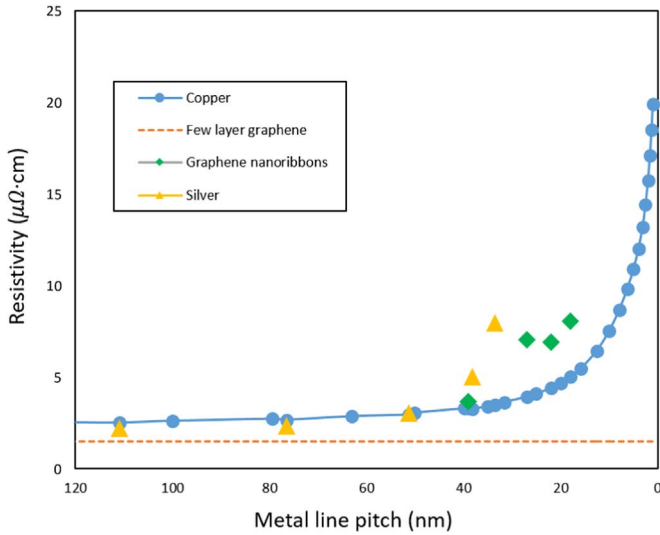


Fig. 1. Interconnect resistivity of different materials versus line width.

The “resistivity wall” phenomenon also leads to a more challenging power network design process due to the significantly resistive local power and ground rails. Reliable and energy efficient power distribution networks are necessary in high performance computing systems [12]. Decreasing supply voltages lead to smaller noise margins. Higher current densities and clock frequencies increase both resistive and inductive power supply noise. Moreover, a primary source of power noise is due to the highly resistive local power metal lines and vias between adjacent metal layers in advanced technology nodes. Poorly or overdesigned power networks either damage the reliability or decrease the performance of integrated circuits. Early assessment of the effects of the structure and material of the power networks supports tradeoffs among power noise, performance, and technology choice.

The rest of this paper is organized as follows. The structure of a typical standard cell based power distribution network is presented in Section 2. A modeling approach is discussed in Section 3. The components of power noise in advanced technology nodes is described in Section 4. Power noise suppression methods are presented in Section 5, followed by some conclusions in Section 6.

2. Standard cell based power network

The structure and impedance characteristics of power grids are presented in Section 2.1. The topology of a standard cell circuit influences the design of the power network, and therefore an overview of the structure is provided in Section 2.2.

2.1. Hierarchy of power grids

The resistance of the power metal lines is affected by the structure of the power grids. An on-chip power grid is a hierarchical structure consisting of a global interdigitated mesh, local power and ground rails, and a via stack connecting the global power grid to the local power rails, as illustrated in Fig. 2. A typical global power grid for high performance ICs uses two layers of orthogonal metal lines to form a mesh structure, as illustrated in Fig. 2(a). Adding global metal layers decreases the grid impedance, reducing power noise in the global power grid. The total number of on-chip metal layers is however limited by the technology. A mesh structure increases the reliability and robustness of a power network due to the multiple redundant paths. The mesh structure also reduces the resistance and parasitic capacitance of the power grids. Each metal layer in a mesh consists of parallel P/G pairs separated from adjacent pairs by tens of micrometers [4]. The pitch of each adjacent P/G pair is a design tradeoff between the

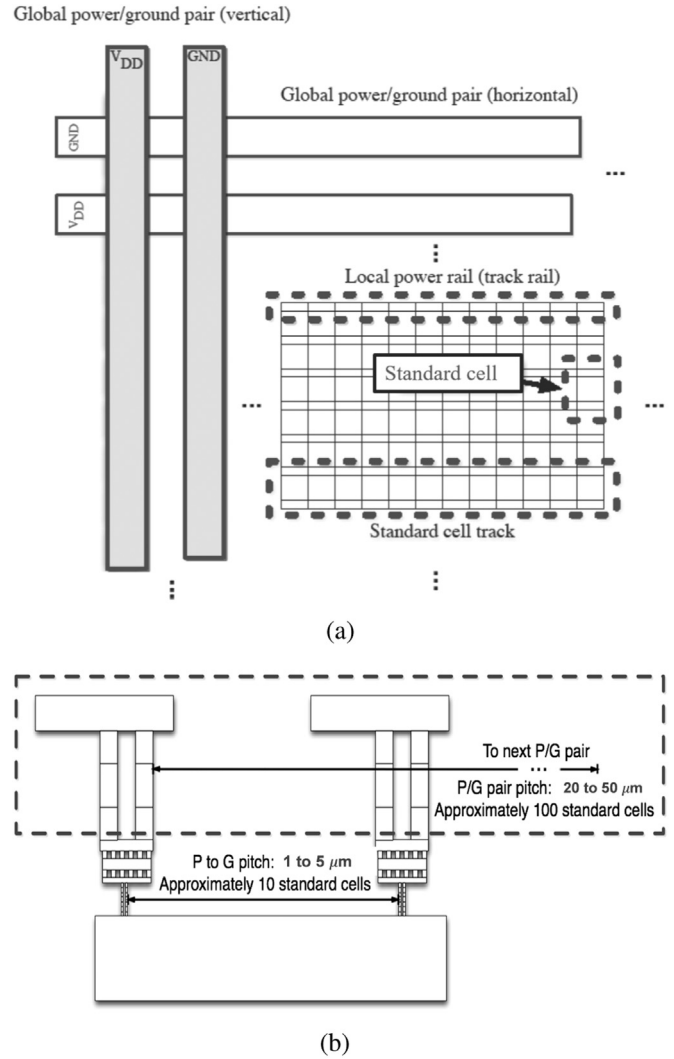


Fig. 2. Topology of a standard cell based power network: a) planar view, b) profile view.

power distribution network and signal/clock routing. The impedance of the global power network typically exhibits low resistance and significant inductance due to the mesh structure. As the current density and clock frequency increases with technology scaling, inductive $L di/dt$ noise becomes comparable to the resistive noise [13,14]. The power noise contributed by the global power grid should therefore be carefully evaluated to satisfy the strict power noise requirements in advanced technology nodes.

2.2. Standard cell based power rails

An individual standard cell track is structured as a row with a substrate region patterned between the power and ground rails, as illustrated in Fig. 2(a). Gates within a cell library are structured to fit within a constant height track with transistors patterned within the substrate. The height of a standard cell is typically controlled by lithographic limits introduced by double and quadruple patterning processes [15]. Standard cell gates are mirrored to ensure that two tracks share a common power rail, doubling the effective current load on the line. After the gates are placed, the interconnections are routed among the internal gates, constraining the available metal resources. The power rail impedances are dominated by the metal resistance and decoupling capacitance. On-chip power noise is caused by current switching on the track rails with the greatest contribution arising from the clocked gates and buffers [16]. Most notably, local power noise is

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