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Analog behavioral equivalence boundary computation under the effect of process variations

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ABSTRACT

Equivalence checking (EC) is a crucial component of integrated circuit (IC) design. EC problem has become even more challenging with the ever-worsening process variations. In our earlier work [10], we researched optimization-based analog equivalence checking (AEC) between Simulink and HSpice models, where we proposed a methodology to find a boundary of equivalence. Although the significance of the effect of process variations is widely accepted, there is limited number of studies addressing the impact of process variations on AEC. In this study, we propose a novel technique to incorporate process variations in AEC. We build a multi-objective optimization problem utilizing evolutionary computation. In this problem, we search for the boundary of equivalence both considering the equivalence value resulting from the effect of process variations and closeness to the boundary. In process variations-effect analysis, we utilize Quasi Monte Carlo (QMC) method to generate samples, which makes it possible to estimate the yield with fewer samples compared to Monte Carlo (MC) method. We generate process variations-aware equivalence boundaries for different equivalence values. We validated our analysis on three designs, an inverter, an operational amplifier, and a buck converter. Our approach proved to be a credible tool for investigating the effect of process variations on the equivalence boundary.

1. Introduction

As feature sizes decrease more and more due to advances in process technologies, nano-scale effects become a problem for designing ICs. There is a continuous need for updating design and manufacturing processes to cope with those effects. Process variation is one of the most important effects in nano-scale design. In addition, time-to-market pressure is another factor whose influence is felt seriously in industrial projects. The largest component of the time spent on industrial integrated circuit projects is the verification of the design. In order to decrease the time spent on verification, simulation times should be decreased and design bugs should be detected at early phases of the project. All these facts necessitate the use of model-based design (MBD), speeding up simulations and enabling the discovery of bugs in early phases. In MBD, functionality of the model should be checked against its implementation in order to ensure the validity of the model and process variations should be taken into consideration.

Methodologies and tools utilized in analog equivalence checking are far from being mature. There is a limited number of studies on analog verification that integrate process variations-effect analysis. In this study, we propose a methodology generating behavioral equivalence boundary under the effect of process variations. We use Simulink as high-level model because it is a widespread design environment for both digital and analog models considering both the availability of numerous built-in functions and its ability to integrate user-defined functions. For the low-level implementation, we use HSpice.

There are various approaches investigating analog equivalence checking (AEC) problem. In [1–4] linearity of analog circuits is assumed and checking is accomplished by comparing linear transfer functions of the specification and the implementation. But transfer function generation is not an easy task and linearization requires manual intervention. Another approach utilized in [5–7] is state space sampling by using non-linear transformations, where difficulty of finding the correct transformations and low possibility of automation affects the soundness of the approach. Another approach is based on input stimuli generation covering the complete state space [8]. Although the approach is reasonable, its applicability is limited by the exponential increase in the run time due to the growth in the number of variables. In order to overcome the state-space explosion problem, we decided to follow an approach similar to [9], which

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presents a hierarchical, optimization based semi-formal (simulation-based) equivalence checking methodology. In that approach equivalence is verified over a constrained input space and the optimization problem is formulated.

We built an analog equivalence boundary search methodology utilizing evolutionary computation in [10]. That evolutionary computation is a modified version of SPEA2 [11]. The approach in [10] is simulation-based and decides equivalence by comparing performance parameters measured from simulations of Simulink model and HSpice netlist for the same input parameters, which characterize the states of inputs. However the approach in [10] does not integrate process variation effects in the analysis.

Process variations were modeled by [12]. Although there is a formal approach to verify analog circuits in the presence of noise and process variation in [13], it is limited to linear time-invariant designs, since it is dependent on the closed form solution for the statistical differential equation (SDE). In [14], again SDE is utilized in verification of analog circuits in presence of noise and process variations using pattern matching. The same limitation of SDE applies here as well and the methodology is limited to fixed simulation step-size.

Two example use cases of our equivalence checking method are its application in analog design and model generation. Considering the analog design flow, the architectural exploration of the design space is more easily performed at the system level. This is achieved by utilization of high level models. However, the accuracy of these models has to be validated before usage. The second usage of our method is for model generation. During the process of model generation, the equivalence of the model to the actual design should be checked under the effect of process variations. By usage of our methodology, designers can be sure about the operation of the model utilized in the system level simulations.

We make the following contributions in this paper:

- We analyze the effects of process variations on AEC, where we generate an equivalence boundary. We investigate the change in equivalence boundary by filtering for different target equivalence threshold values.
- We utilize evolutionary computation in our process variations-aware AEC analysis.
- We apply Quasi Monte Carlo (QMC) method in process variations-effect analysis, which makes it possible to estimate the yield with fewer samples compared to Monte Carlo (MC).
- We build a multi-objective optimization problem, where in addition to equivalence value, we consider closeness to the equivalence boundary by defining a parameter for each point of concern.
- We demonstrate the validity of our approach on three designs, an inverter, an operational amplifier and a buck converter.
- We utilize Simulink and HSpice only for validating the proposed approach. The overall approach is independent of them, any high level model and any circuit simulator can be used in our process variations-effect analysis.

The paper is organized as follows. In Section 2, we present our methodology following its flow graph. In Section 3, we present the applications of our methodology on three examples: Inverter, Operational Amplifier and Buck Converter and provide the results of those applications. In Section 4, we discuss the results of the experiments. In Section 5, we define future work to be done and conclude the paper.

2. Methodology

In this section, we first describe our approach to check analog equivalence and explain our process variations-effect analysis for analog behavioral equivalence boundary computation. Then we define the inputs of our analysis and explain the details of each step in the analysis in subsections.

To perform equivalence checking we utilize a set of performance and input parameters for high-level (Simulink) and low-level (HSpice) designs. *Performance parameters* capture the essential characteristics of designs during their simulation. Some typical performance parameters are propagation delay, slew rate, and output voltage. *Input parameters* characterize the state of the inputs to the design, e.g., rise time of the input voltage, input voltage value, and parasitic resistances. In our approach, we simulate Simulink model and HSpice netlist with different input parameters and measure performance parameters from those simulations. We decide analog equivalence by comparison of those performance parameters.

The goal of our methodology is to determine the effect of process variations on the equivalence boundary of input parameters. To reach that goal, the difference between the performance parameters of the models being below a given threshold is defined as our success criteria. We use a user-defined *success threshold* because analog signals cannot be exactly identical. Hence, we can determine the regions, where both designs are equivalent to each other within a tolerance value under the effect of process variations.

Now we describe our process variations-effect analysis for analog equivalence boundary computation, which is shown in Fig. 1.

2.1. Inputs of analysis

We perform process variations-effect analysis on an equivalence

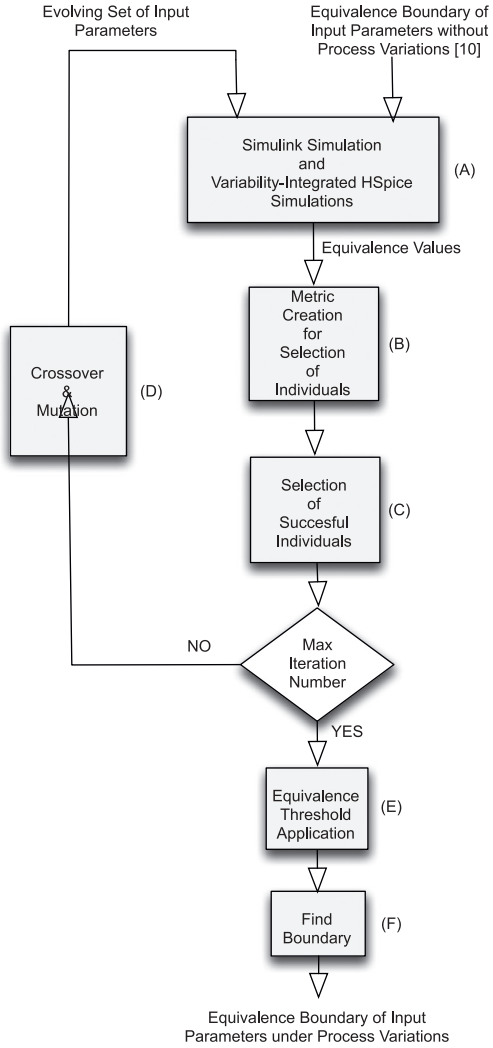

Fig. 1. Flow diagram for process variations-effect analysis for analog behavioral equivalence boundary computation.