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Detailed placement for pulse quenching enhancement in anti-radiation combinational circuit design

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ABSTRACT

Pulse width of single event transient can be shrunk by pulse quenching effect in combinational circuits. And it is found that the pulse quenching effect is closely related to the layout of the circuits. In this paper, we propose a placement method for reducing soft errors in combinational circuits by increasing the number of quenching unit and enhancing the pulse quenching effect between them. To evaluate the soft error automatically, an evaluation platform is also implemented and embedded into commercial EDA tools with our placer. Simulation results show that our proposed method can reduce the soft error vulnerabilities by 14%–26%.

1. Introduction

Anti-radiation integrated circuit is one of the key technologies in the electronic system of all kinds of spacecraft. Space particles striking the integrated circuit will produce a variety of radiation effects, such as single event effect (SEE), accumulation effect and displacement damage [1]. SEE is one of the main failure modes of the electronic system in the space radiation environment. It includes single event upset (SEU) and single event transient (SET). Both SEU in sequential logic unit, and SET captured at the end of the combinational circuits will lead to soft errors. With the decreasing of the capacitance of the node, the shortening of the pitch, and the increasing of the clock frequency, SET in the combinational circuits become the main source of the soft errors at the nanometer scale. Therefore, more attention should be paid to the soft error evaluation and the radiation hardening technology for the combinational circuits.

In deep submicron CMOS technology, the collection of the charge on multiple circuit nodes which is deposited by a single particle strike can thwart conventional soft error hardening schemes employed in many CMOS platforms [2]. Multi node charge sharing caused by a single event may lead to multiple single-event transient (MSET), and it may also generate pulse quenching effect, which has great influence on the soft error analysis and hardening [3,4]. Both MSET and pulse quenching effect may have unpredictable effects on the circuit's radiation resistance [5], which is depended on the structure, cells location, timing characteristics, parasitic and other factors. For example, when MSET occurs, transient pulses propagating in multiple paths may cause reconvergence or more soft errors; while pulse quenching effect may shrink or even cut off the pulse width under certain conditions [5]. Consequently, it becomes complicated to analyze the soft error rate of the combinational circuits in the nano-technology.

Because charge sharing effect is more likely to occur under advanced manufacturing processes and the proportion of soft errors occurring in combinational circuits is increasing, it arouses more attention in reducing soft error rate (SER) in combinational circuits. The charge sharing effect is directly affected by the electrically related relationship and the distance between the physically adjacent cells. Therefore, it is feasible to enhance the pulse quenching effect and reduce soft error by changing cell locations during placement. In Ref. [6], cells in circuit are divided into good/bad pairs according to pass/fail value of all possible pairs of nodes in circuit, and then an annealing algorithm is applied to maximize the number of good pairs. The number of simulated gate pairs is C_n^2, where n is the number of nodes. The result shows that the runtime increases rapidly with the size of the circuit growing. The runtime will be unacceptable when the method is used to large scale circuit design. In Ref. [7], the sensitivity of each pair nodes is calculated, and the SET produced between the nearby nodes with high sensitivity has a higher probability to be masked. According to the sensitivity information, a set of placement constraints is built and converted to the bounding commands. These commands are added into the simulation script used by electronic design automation (EDA) tools to place high sensitive nodes as closed as possible. This method takes advantage of commercial EDA tools, but it not automated and not flexible enough. The pulse quenching effect can be

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enhanced by adjusting the directions and locations of the cells [3,8]. In Ref. [9], a novel constrained layout placement approach is proposed to reduce the soft error vulnerabilities by enlarging the number of quenching units and decreasing the distance between them. Yet these three works are all about modifying circuit layout to reduce soft error vulnerabilities. They are effective but not easy to use in other cases. Actually, these works have not use placement algorithm at all. In Refs. [10] and [11], authors treat longer interconnects as a low pass filter for glitches induced by radiation strikes, and show that it can be used to optimize the circuit SER during placement. Pulse quenching effect not only makes it possible to reduce soft error in combinational circuit, but also makes it difficult to evaluate the SER. To trade-off between efficiency and accuracy, the difference of SER is analyzed when considering pulse quenching effect [12,13], and a mixed-mode method combined with an academic fast propagation algorithm and commercial HSPICE tools is provided in Ref. [14].

The contributions of our work are summarized as follows.

- Present a placement method for both pulse quenching effect enhancement and soft error rate reduction.
- Give a placement and evaluation platform which can be used independently, or be used with commercial EDA tools. This platform is extensible and can be applied to practical engineering.
- Compared with the previous work, our placement method is more automatic and scalable. The complexity of our algorithm is between $O(n)$ and $O(n^2)$. We also consider the tradition optimization target to achieve the balance of wire length, density and anti-radiation performance.

The rest of this paper is organized as follows: Section 2 introduces the conditions of pulse quenching effect and influencing factor. Section 3 provides an overview of the placement method to enhance pulse quenching effect in combinational circuit firstly, and then gives the details of soft error reducing algorithms. Section 4 introduces the soft error reducing placement and evaluation platform. Section 5 presents the simulation results. Finally, Section 6 gives the conclusions of this paper.

2. Preliminary

Pulse quenching effect is a special situation of charge sharing effect, it occurs when connected cells collect charge at the same time. In Fig. 1(a), a pair of connected cells *a* and *b* are in the same row and next to each other. Suppose both *a* and *b* are inverters(shown in Fig. 1(b)). The input to the *a* is HIGH, and the output of *a* is LOW. Then the pMOS transistor associated with *a* is OFF, and the pMOS of *b* is ON. When cell *a* is struck, it will produce a LOW-HIGH transient which turns the pMOS of *b* to OFF. When the pMOS of *b* turns OFF, it becomes susceptible to collect charge. The charge sharing signal generated at *b* prematurely forces the output back to HIGH stage. Then the pulse at output of *b* is truncated [5]. The waveform is shown in Fig. 1(c). Ion strike causes a positive impulse in *a*, and a reverse impulse in *b*. Finally, the pair of *a* and *b* exports a narrowing transient.

In Fig. 1(a), *dist* is the distance between *a* and *b*. When pulse quenching effect occurs, the pulse width at the output of *b* is dependent on dist. In order to obtain the exact relation between distance and quenching effect, we use Synopsys TCAD tools to simulate the different

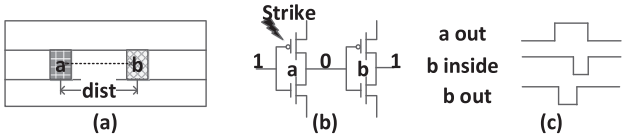

Fig. 1. An example to show quenching unit in circuit layout (a). A schematic of two inverters illustrating the pulse quenching effect (b). The waveform influenced by the pulse quenching effect (c).

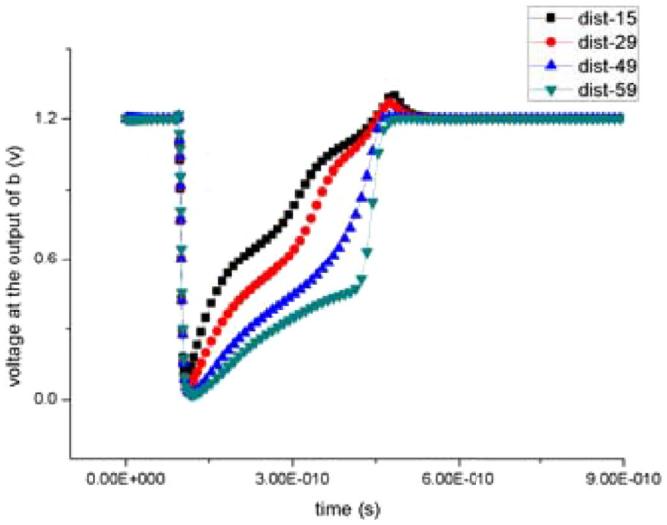

Fig. 2. Relationship between pulse quenching effect and distance of neighboring cells.

cases. During the simulation, LET is set 30 *MeV ·cm2/mg*, and strike location is set at the center of drain region of cell *a*. The result of Fig. 1 is shown in Fig. 2. It shows the voltage at the output of *b* with time in different cases. The width of the transient pulse varies with *dist*, it is found that the smaller the *dist* is, the more obvious the pulse shrinks. When the *dist* is large enough, the pulse quenching effect vanishes.

Three conditions are required for occurrence of the pulse quenching effect: electrically related relationship, physically adjacent position, and appropriate voltage stage. During the placement process, the structure of circuit is not changed, and the voltage stage of each cell is related to the input stimuli. In this paper, we focus on the relative position between the connected cells, and try to enhance the pulse quenching effect during the placement stage. The details of our technologies will be introduced in in Section 3 and Section 4.

3. Placement strategy

Generally speaking, the placement process includes three steps: global placement, legalization, and detailed placement. The global placement process plays an important role in improving the quality of the layout. The goal of legalization process is to eliminate the cells overlap and approximate minimize the total wire length. The detailed placement process further improves timing, wire length and density of layout. In recent year, many works have focused on the global placement. Some global method have been proposed such as analytical placement [15,16], force-directed placement [17], partitioning-based approach [18], simulated annealing-based approaches [19] and electrostatics-based placement [20]. As to detailed placement, the most well-known methods are mPL6 [15], NTUPlace [16] and FastPlace-DP [21]. In Ref. [22] the author proposed a mixed integer programming models to optimize detailed placement [23]. proposed a routability-driven placement optimizer that can improve the placement solution in terms of wire-length and routability. Ref. [24] proposed a timing-driven placement method based on dynamic net-weighting. In this paper, our placement strategy focuses on detailed placement process, and the input layout is generated by Cadence Encounter.

3.1. Overview

In our placement, the quenching unit (QU) is defined as two adjacent cells *a* and *b* in the same row and electrically related, and the precursor cell of cell *a* is the cell connected to the input pin of cell *a*, and the successor cells of cell *a* is the cells connected to the output pin of cell *a*.