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Metastability immune and area efficient error masking flip-flop for timing error resilient designs

Govinda Sannena*, Bishnu Prasad Das

Department of Electronics and Communication Engineering, Indian Institute of Technology, Roorkee, India

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ABSTRACT

Reducing the worst case timing guard bands is one of the major concerns in high performance designs with limited power budget in the advanced nano-scale technology nodes. In this work, an error masking flip-flop is proposed to reduce the worst case timing guard bands by detecting and correcting timing violations. It consists of a pulse generator, an error detector and a multiplexer along with a conventional flip-flop. Exploiting an intermediate multiplexer between master and slave latch of a conventional flip-flop, the erroneous output state of the flip-flop due to timing violations is corrected by providing direct data to slave latch. The proposed flip-flop occupies 16% less area compared to error masking flip-flops available in literature. A core level clock gating is employed for error recovery which shifts the rising edge of the clock by one period in case of a timing violation. ISCAS'89 benchmark circuits, a 32-bit pipelined adder and a 16-bit pipelined multiplier are implemented in 130 nm technology, which use error masking flip-flop for dynamic voltage and frequency scaling (DVFS). It is shown that using error masking flip-flops with DVFS can either reduce power consumption up to 20% or improve the performance up to 32% in typical operating conditions compared to worst case design.

1. Introduction

CMOS technology scaling has enabled digital integrated circuits to achieve higher performance with better energy efficiency. However, increased process, voltage and temperature (PVT) variations with technology scaling cause significant variation in the performance of the design in deep sub-micron (DSM) technologies. Moreover, transistor aging due to bias temperature instability(BTI) degrades the performance of the design with time. Voltage or timing guard bands are added to nominal voltage or frequency to cope with these worst case PVT variations [1–3]. However, these worst case operating conditions occur with less probability. Guard bands added to tolerate the variations, either increase the power consumption or limit the performance in typical conditions. Additionally, large guard bands are required below 65 nm technology, motivating to implement variation aware adaptive design methodologies.

Timing error resilient techniques operate the design below critical supply voltage or above the maximum operating frequency under typical operating conditions. The critical supply voltage or maximum operating frequency of the design are determined based on worst case conditions. Error detection and correction(EDC) or error masking flip-flops are used to detect occasional timing violations occurred because of operating at reduced supply voltage or increased frequency. EDC techniques proposed in [1–6] use either double sampling [1] or transition detection [3] approaches to detect timing violations. These techniques use counterflow pipelining [1] or instruction replay mechanisms [4] to error recovery. Counterflow pipelining and instruction replay mechanisms will reduce throughput of the design as they need $2k$ and $3N$ clock cycles respectively to correct the erroneous state, where k is the order of the pipeline stage that flags a timing error and N is number of pipeline stages [7]. For higher timing error rates, the throughput of the design is reduced drastically because of error correction. Moreover, these techniques correct timing violations using instruction replay mechanism which is available in processor architectures. One cycle correction method proposed in [7], increases the throughput of design but requires large area overhead as all the flip-flops in a pipeline stage are needed to be replaced with EDC flip-flops even if one critical path exists in the pipeline stage.

Error prediction techniques proposed in [8–13] monitor delayed data to predict possible occurrence of timing violation. As flip-flop output is always correct, these techniques do not incur correction overhead. On the other hand, error masking techniques detect the timing violations and correct the erroneous output state of the flip-flop in the same clock cycle. In these techniques, timing errors are corrected by using time borrowing property similar to that of latch based designs. The next pipeline stage may need extra time for logic evaluation as the

* Corresponding author.
E-mail address: govinda.sannena@gmail.com (G. Sannena).

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corrected outputs are available after some error masking delay. The clock stretching technique [14,15] or clock gating [16] can be used to recover from timing errors. In [17], a positive latch is used in the data path instead of flip-flop to avoid metastability in data path. Timing error prevention technique in [14] uses pulsed latches and clock stretching. The time borrowing property of latch is used in these techniques to correct timing errors.

TIMBER flip-flop in [18] compares the output of master latch with that of shadow latch. The shadow latch uses a delayed clock and error relay logic is used to determine required delay. Moreover, a metastable detector is needed as master latch output may become metastable if there is concurrent data and clock transitions [1]. This technique incurs large area and power overhead because of metastable detector and error relay logic. A dynamic flip-flop conversion (DFFC) method has been proposed in [19] which is based on time borrowing. In this, the master latch clock is modified after detecting a timing violation at half way point so that it becomes transparent. This method suffers from false error detection. Variants of [19] have been proposed in [21,20], which solves the false error detection problem and improves the performance of the design. However, the area and power overhead due to timing violation predictor and data arrival detection block increase with number of critical paths of the design. Moreover, half way point selection becomes very complex with increased process variations.

An error masking technique in [22] uses bit flipping concept. The input and output of the flip-flop are compared using an XOR gate to detect timing violations. A pulsed latch is used to store the error signal. The pulse latch clock should maintain a delay of worst case clock-to-Q delay to avoid false error detection. An XOR gate complements the output of the conventional flip-flop in case of timing violation. This technique also uses a metastable detector. Data path glitches lead to a glitch on the error signal.

Error resilient flip-flop in [23] detects timing violations by comparing the master latch output with the input. A multiplexer is used to correct the erroneous output. Either the master latch output or flip-flop input drives the slave latch depending on the error signal. The late arrival detector utilizes master latch internal nodes. However, the intermediate nodes may enter into metastable state in case of concurrent clock and data transitions [1]. In this case, intermediate nodes of master latch resolve to either logic '1' or logic '0'. Data transitions which cause metastability at the intermediate nodes may not be detected as errors using late arrival detector.

Error masking flip-flops in [24] detects timing violations by monitoring delayed data. The timing violations are corrected using either asynchronous preset and clear or uses an extra circuitry to make the master latch transparent. Flip-flop output is corrected by feeding the direct input data to slave latch through master latch in case of timing violation which significantly increases error masking latency which in turn reduces energy savings.

In this work, an error masking flip-flop has been proposed. The preliminary version of this work is published in [25]. The major contributions of this work are:

1. A system level implementation of the proposed flip-flop is presented to explain the usage of the proposed flip-flop. The system level implementation includes a set dominant latch and a clock gating controller for error recovery. The circuit level implementations of set dominant latch and clock gating controller are different from the existing techniques in the literature.
2. The proposed flip-flop is analyzed in detail for the data path glitches and metastability.
3. The proposed flip-flop is employed in ISCAS'89 benchmarks to evaluate the energy savings in dynamic voltage and frequency scaling (DVFS) applications compared to worst case designs. The benchmark circuits are implemented in industrial 130 nm CMOS technology with a nominal supply voltage of 1.2 V.

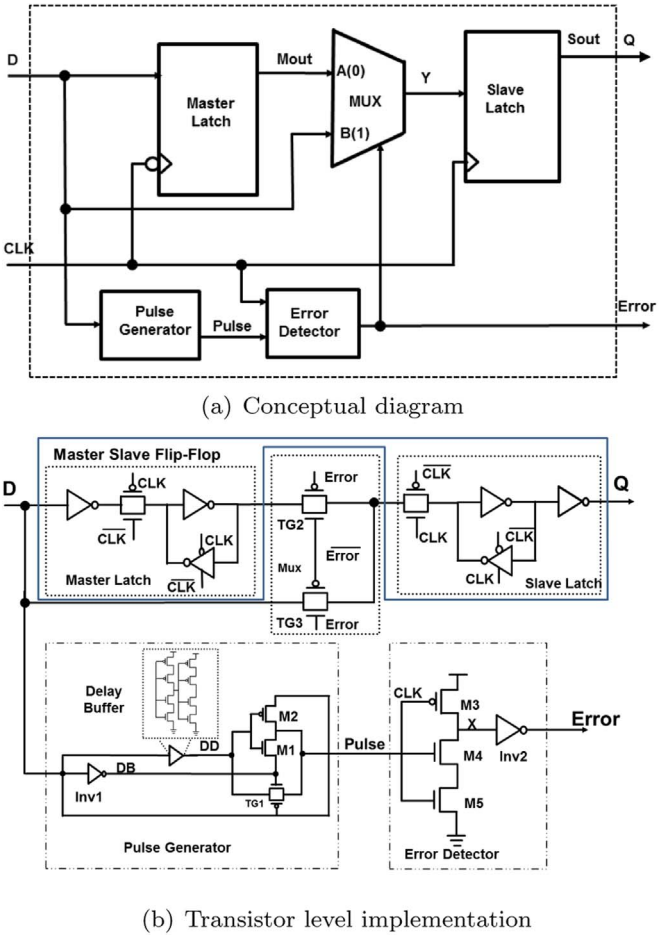

Fig. 1. Proposed flip-flop.

4. The simulation flow to find the minimum operating voltage or maximum operating frequency of design by employing proposed FF along with DVFS is presented.

This paper is organized as follows. The operation of proposed error masking flip-flop is described in Section 2. The system level implementation is presented in Section 3. The timing analysis of the design in the presence of error masking flip-flops is explained in Section 4. The simulation results are discussed in Section 5. Finally, this work is concluded in Section 6.

2. Proposed error masking flip-flop

The proposed timing error masking flip-flop (EMFF) employs an input data transition detection scheme to monitor late arrived signals due to variations. It consists of a master latch, a slave latch, a 2:1 multiplexer, a pulse generator and an error detector. Master and slave latches are transparent during low and high phases of the clock respectively. The circuit diagram of the proposed flip-flop is shown in Fig. 1. A data transition at the *D* input of the master latch results in a pulse at the output of pulse generator. Error detector flags an *Error* signal when both clock and output of the pulse generator are at logic high. When a setup time violation occurs, the *Error* signal becomes logic high. In case of timing violation, master latch samples incorrect data and the erroneous output is corrected by driving the slave latch with *D* signal using the multiplexer instead of master latch output. The correct data should be appeared at the output of the slave latch before it becomes opaque to data transitions.