Integration, the VLSI Journal xxx (2017) 1–12

Contents lists available at ScienceDirect

Integration, the VLSI Journal

journal homepage: www.elsevier.com/locate/vlsi

High-performance and energy-efficient 64-bit incrementer/decrementer using Multiple-Output Monotonic CMOS

Dimitrios Balobas *, Nikos Konofaos

Department of Informatics, Aristotle University of Thessaloniki, 54124 Thessaloniki, Greece

ARTICLE INFO

Keywords:
64-Bit incrementer/decrementer
Energy-efficient
High-performance
Multiple-Output Monotonic CMOS

ABSTRACT

In this paper, we introduce the Multiple-Output Monotonic CMOS (M^2CMOS) logic style, which is applied on the design of a high-performance and energy-efficient 64-bit incrementer/decrementer circuit. M^2CMOS is proposed as an enhancement to standard monotonic-static logic and a viable alternative to domino logic for high-performance applications. A simulation-based comparative analysis at the 32 nm concludes that, compared to other state-of-the-art designs, the proposed incrementer/decrementer achieves the best results in terms of gate/transistor count, delay, energy-delay-product and standby power.

1. Introduction

A digital circuit that increases (decreases) an N-bit binary number by 1 is called an incrementer (decrementer). Incrementing an input word can be defined as finding the least significant zero bit (LSZB) in the word and inverting all the bits up to that point, whereas decrementing can be defined as finding the least significant one bit (LSOB) and then inverting all the bits up to that point [1]. Due to the similarity of these procedures, both functions can be combined in the same circuit, which is called an incrementer/decrementer (Inc/Dec). Conventional implementations of the CMOS Inc/Dec involve adding/subtracting 1 to an input word, by utilizing the adder/subtractor. Nonetheless, several implementations of specialized Inc/Dec circuits have been proposed with different design techniques and performance tradeoffs [2–9].

Hashemian [2] proposed a highly parallel 64-bit Inc/Dec in 3 μm CMOS using 3 types of logic blocks: a NAND-NOR network, priority resolution modules and selector modules. The circuit's implementation used static/dynamic logic and a novel CMOS staircase technique. Hashemian and Chen [3] combined Inc/Dec and 2's complement functionality in the same circuit, which was also implemented in 3 μm CMOS with a reported maximum delay of 14 ns.

Huang et al. proposed high speed 32-bit [4] and 64-bit [5] Inc/Dec circuits in 0.6 μm using NP-domino logic combined with the multilevel lookahead [4,5] and multilevel folding [5] techniques. The architecture of the Inc/Dec was separated into three modules: input selector, decision logic and output selector. In Ref. [5], the 64-bit Inc/Dec with multilevel lookahead/folding reportedly achieved a delay of 3.14 ns, being 26% faster than the one implemented with only the multilevel lookahead and 70% faster than a conventional implementation based on the carry-select adder. Fig. 1 illustrates a block diagram of the 64-bit Inc/Dec with the multilevel lookahead/folding architecture, as proposed in Ref. [5].

Bi et al. [6] proposed a 32/64-bit MUX-based Inc/Dec which used a similar three-module architecture with ripple carry structure for decision logic. Veeramachaneni et al. [7] added 8-bit lookahead structure to the 32-bit circuit of [6] and claimed 47% and 38% improvements in delay and energy respectively. All the reported delays in Ref. [6] (FPGA-based) and [7] (0.18 μm CMOS) exceeded 10 ns. Fig. 2 illustrates the architecture of an N-bit MUX-based Inc/Dec, implemented with 2-input static CMOS gates, as proposed in Ref. [7].

In more recent works [8,9], two low-power 32-bit Inc/Dec circuits were developed in 0.25 μm, using static CMOS for lookahead logic and multiple-output domino logic (MODL) for 8-bit Inc/Dec blocks. Archanadevi et al. [8] used a LSOB-based approach with a reported 25–30% reduction in power compared to [5]. Balasubramanian and Mastorakis [9] used an improved LSZB-based approach with a reported power reduction of 61.4% and 55.7% compared to [5] and [8] respectively. Fig. 3 illustrates the architecture of an N-bit LSZB-based Inc/Dec, as proposed in Ref. [9].

This work presents a novel 64-bit CMOS Inc/Dec with a full-custom design at the transistor level, incorporating a new design technique. An extensive simulation-based research is conducted at 32 nm, in order to evaluate the proposed circuit against the state-of-the-art [5,7,9]. The rest of this paper is organized as follows. Section 2 provides an overview of the monotonic-static logic family followed by an analysis of the new

* Corresponding author.
E-mail addresses: dmpalomp@csd.auth.gr (D. Balobas), nkonofao@csd.auth.gr (N. Konofaos).

https://doi.org/10.1016/j.vlsi.2018.03.013
Received 5 September 2017; Received in revised form 3 March 2018; Accepted 18 March 2018
Available online xxxx

Please cite this article in press as: D. Balobas, N. Konofaos, High-performance and energy-efficient 64-bit incrementer/decrementer using Multiple-Output Monotonic CMOS, Integration, the VLSI Journal (2017), https://doi.org/10.1016/j.vlsi.2018.03.013

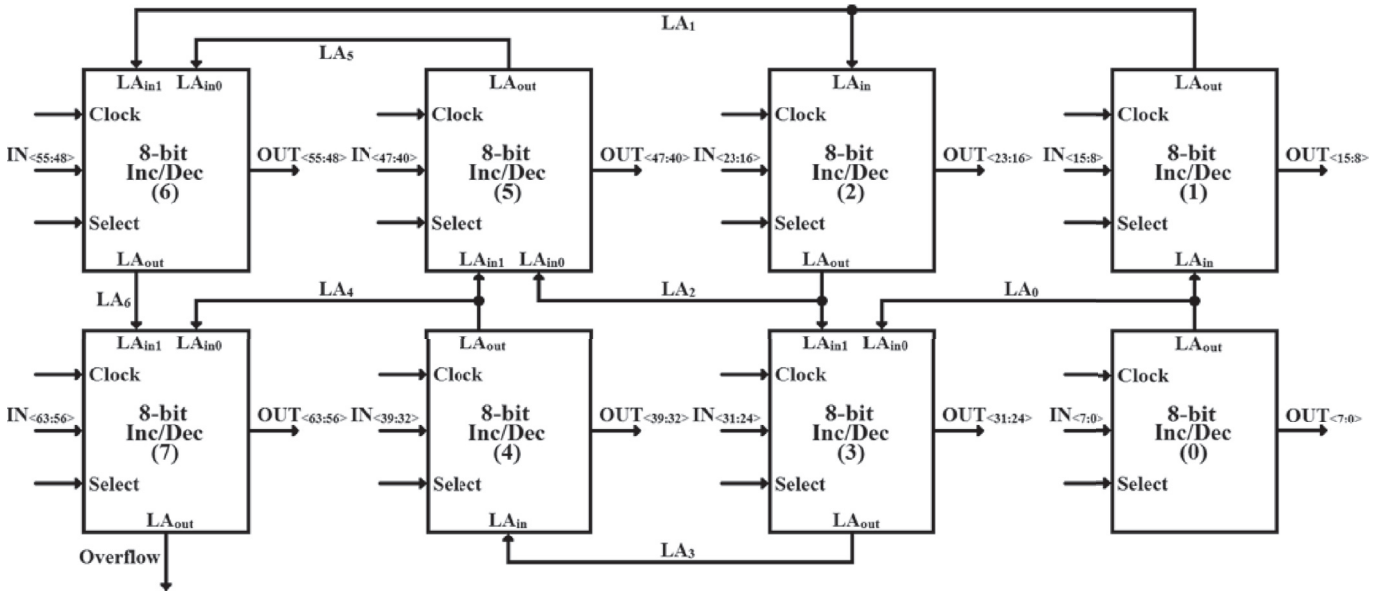

Fig. 1. 64-bit Inc/Dec with the multilevel lookahead/folding architecture [5].

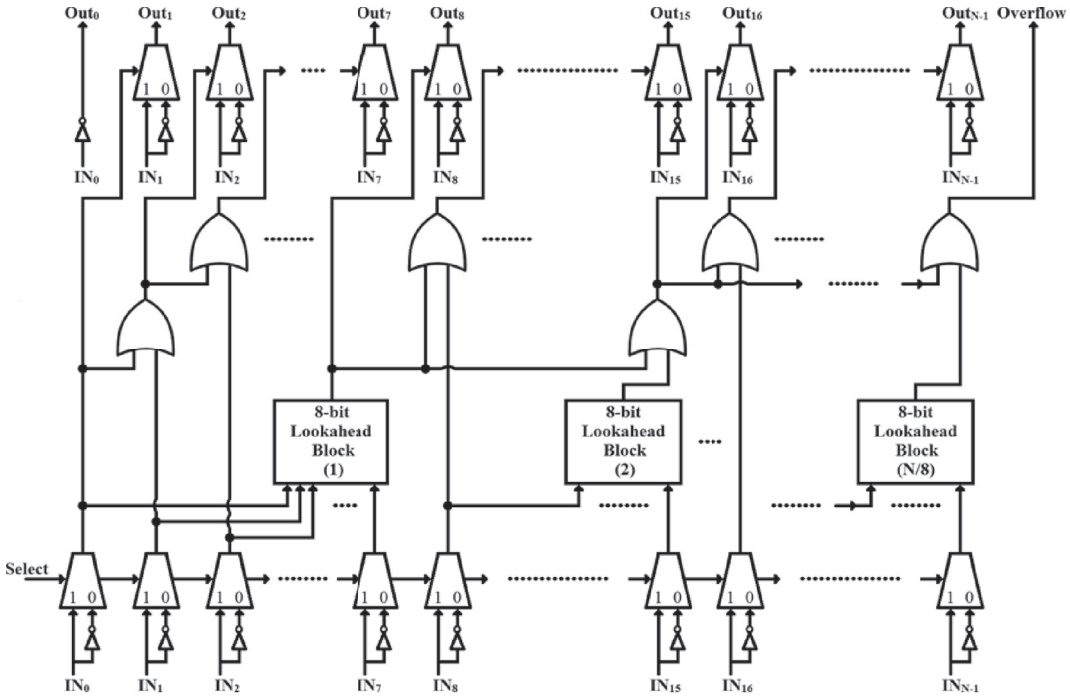

Fig. 2. N-bit MUX-based Inc/Dec [7].

technique. Section 3 presents the new 64-bit Inc/Dec architecture. Sections 4 and 5 provide the simulation setup and corresponding results of our comparative analysis respectively. Finally, the conclusion is drawn in section 6.

2. Monotonic static CMOS logic

2.1. Characterization

Monotonic static CMOS (MS-CMOS) [10–16] is a static/dynamic hybrid logic family which seeks to combine the robustness of static CMOS with the high performance of dynamic circuit techniques. Its logic operation is clocked and segregated in precharge/evaluation cycles similarly to dynamic logic, but it keeps both complementary nMOS and pMOS logic networks, similarly to static CMOS.

In static CMOS logic, gates are often designed to achieve equal rise/fall times, with proper sizing of the complementary networks [1]. MS-CMOS gates, on the other hand, are monotonic in nature and thus they are usually skewed to favor either one of the two possible transitions (high-to-low or low-to-high). With proper design and sequencing, MS-CMOS gates will always perform their favored transition during evaluation, improving the overall performance. Their weak logic network only serves as a complex keeper to fight leakage and noise during precharge phase. The concept of complex keepers was introduced by Noise-Tolerant Precharge (NTP) logic [17,18], which utilizes n-type domino gates with full complementary networks of weak pMOS and can