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A novel design of a ternary coded decimal adder/subtractor using reversible ternary gates

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ABSTRACT

In recent years, an outstanding amount of interest has been given to reversible circuits. Their applications in distinctive fields that include digital circuit design with low-power consumption, computational circuit design in quantum computer and DNA-based computations are of high significance. Because of advantages of ternary circuits over binary circuits, such as reducing the complexity of interconnects, smaller chip area and reducing the number of quantum cells for the quantum circuit, ternary logic is suggested to construct new compact circuits. Also, in quantum technology, without any restrictions with the same physical phenomena that binary circuits are implemented, new circuits can be implemented in ternary logic. Circuit design for decimal calculations, which includes addition and subtraction of decimal numbers, has continually been the interest of digital circuit designers. In reversible ternary computation, the reversible circuits for decimal calculations have been less studied. In this paper, a reversible ternary adder/subtractor circuit for the addition/subtraction of decimal digits in radix three is proposed. Ternary Coded Decimal (TCD) codes are used to display decimal inputs and outputs. In circuit implementation, first by removing the unused inputs and outputs in the required ternary adders in the TCD Adder, three blocks of reversible 3-qutrit ternary adder with the quantum cost of 29, 22, 14 and constant inputs of 0, 1, and 0 were presented, then an optimal circuit for the TCD detector with a quantum cost of 16 was introduced. The proposed TCD detector has 23% improvement in quantum cost as compared to the existing design. By applying these in the design of the reversible TCD Adder, a more optimal reversible TCD Adder circuit than the existing design was presented resulting in a 31% improvement in quantum cost and 58% improvement in the number of constant inputs. Finally, decimal 9's complement circuit for the subtraction of two decimal numbers was proposed. In the proposed TCD Adder/Subtractor, the new proposed TCD Adder and decimal 9's complement circuits were used. To realize all proposed circuits, 1-qutrit shift gates and 2-qutrit Muthukrishnan-Stroud gates, which are realized in ion-trap technology in quantum computers, were used.

1. Introduction

In the last few years, reversible computing has received much attention and has become one of the emerging important technologies. In 1960, Landauer [1] proved that using irreversible logic in computation would dissipate *KTLn*2 joules of heat energy for each bit of information lost. (K is referred to Boltzmann's constant and T is the absolute temperature at which computation is performed). Nowadays, energy dissipation is an important issue in modern technologies such as low-power VLSI designs [2,3]. Reversible logic is focused on as a special class of quantum computing that implements unitary functions [4]. Any unitary operation is reversible; hence, reversible logic must be used to design quantum circuits. In 1973, Bennet [5] proved that if a computation were performed in a reversible logic, energy would not be dissipated. Bennet showed that if a technology were based on reversible logic, the energy consumption could be as low as possible in theory. If an algorithm could run backward, then it could be called a reversible algorithm [6]. Reversible circuits (gates) have the same number of inputs and outputs, and the input vector states are uniquely reconstructed from the output vector states [7,8]. The constraints in designing reversible circuits are fan-out free and feedback free. Therefore, the reversible circuit design is more difficult than the design of the irreversible digital circuit [9]. Recently, because of the increasing number of inputs and outputs in integrated circuits and

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also reducing the physical size of integrated circuit implementation, the digital circuit design has become more complicated. Multi-valued logic is used instead of binary logic as the solution for this issue [10,11]. In multi-valued logic, the logic of the three values (Ternary) are emphasized [12]. Designing quantum circuits with reversible ternary gates, compared with reversible binary gates, can reduce quantum cells; thus, the result will have better performance and higher speed [13].

The binary logic system only uses 0 and 1 digits, whereas, in ternary system 0, 1 and 2 digits are used. The qutrit is referred to the quantum ternary digit in the ternary quantum computer. A qutrit quantum computer design is presented in Refs. [14–16]. If using a ternary system in comparison with a binary system, in the same N-dimensional space, 37% of qutrit is less used than qubit. So logical functions designed in ternary logic will be 37% more compact [17]. Different designs for ternary reversible circuits have been proposed in the literature. Reversible ternary adder suggested in Refs. [11,17–20] and comparator circuits are presented in Refs. [21–23]. The performance of ternary circuits for quantum/reversible computing refers to the number of M-S (Muthukrishnan and Stroud) and shift gates. M-S gate is a primitive gate in quantum/reversible ternary computing, which is implemented in liquid ion trap quantum technology [14]. M-S gates are the implementation of controlled-Not among qutrits in Ternary logic. The reversible ternary circuit design can be performed by a sequence of 1-qutrit shift gates and 2-qutrit M-S gates.

Consistent with its financial and commercial applications, the decimal computing is important. Another reason for considering the decimal computing is that all decimal numbers cannot be accurately expressed by binary numbers. Therefore, it cannot be stated that the decimal arithmetic result will always be the same as binary arithmetic result equivalent. Typically, the decimal computation is performed on binary hardware using emulation software that is accompanied by the mathematical approximations. Therefore, the use of binary circuits for decimal computation makes the calculation process slow. Accordingly, higher efficiency will be obtained if the hardware designed for decimal arithmetic is used. With the increased demand for decimal arithmetic, reversible decimal adder/subtractor has also been introduced in various research works by using BCD codes [24,25]. Ternary coded decimal (TCD) codes similar to binary coded decimal (BCD) codes are used for coding decimal digits to ternar y digits.

In this paper, for the first time, we have proposed a novel design for reversible ternary decimal adder/subtractor circuit which uses Ternary coded decimal (TCD) codes. Recently, the design of TCD Adder is suggested by Haghparast et al. [17]. In this paper, new circuits for the TCD Adder and TCD Adder/Subtractor are presented. Our proposed TCD Adder is more efficient than the proposed circuit in Ref. [17]. In the design of the TCD Adder/Subtractor, three new blocks of reversible 3-qutrit ternary adder have been used, so that, the unused inputs and outputs are eliminated for the application of each block in TCD Adder/Subtractor. In addition, the circuit proposed for the invalid TCD detector is more efficient than the equivalent circuit in Ref. [17] and has a fewer gate number. All proposed circuits are realized with ternary 1-qutrit shift and 2-qutrit M-S gates.

The structure of the paper is as follows: Section 2 presents the basic concept of reversible ternary logic and basic reversible ternary gates that will be used in the following sections to design the proposed reversible ternary circuits. Ternary coded decimal (TCD) codes are introduced in section 3, and in this section, the decimal addition and subtraction using TCD codes are explained. Section 4 presents the realization of proposed reversible ternary circuits. First, we propose three blocks of the reversible 3-qutrit ternary adder; and then, the circuit of TCD detector and TCD Adder are proposed. Finally, we propose new circuit for reversible TCD Adder/Subtractor. In Section 5, the evaluations of the obtained circuits are discussed. The conclusion of our work is presented in Section 6.

2. Preliminaries

In this section, the basic concepts and comparison parameters for the reversible ternary circuits and binary circuits are first reviewed, and then, the reversible ternary gates that are used in the design of the circuits proposed in the later sections are explained.

2.1. Basic concept

Ternary logic is the generalization of the binary logic and cannot use boolean structure. A ternary logic system was first proposed by Jan Lukasiewicz in 1920, as the generalization of the classical binary logic [26]. After that, Lukasiewicz proposed the multi-valued logic. Lotfi Zadeh introduced the Fuzzy set theory in 1965 [27]. Both, multi-valued and Fuzzy logic have the same rules. The reversible ternary logic circuit, similar to the reversible binary circuit, is an efficient design with a minimum number of garbage outputs, minimum quantum cost and a minimum number of constant inputs.

Garbage Outputs: The garbage outputs in a circuit include logical functions which are not used or expected by the designer as the approved outputs. Consistent with the fact that in reversible circuits the number of inputs and outputs should be the same, garbage outputs are added to maintain the reversibility in the circuits. In reversible binary circuits, the values of garbage outputs are equal to 0 or 1, while in reversible ternary circuit, the values can be 0, 1 or 2.

Constant Inputs: In reversible ternary circuits, the constant inputs refer to the number of inputs which must be constant at 0 or 1 or 2 in order to achieve the desired reversible logic functions, while in the reversible binary circuits, constant inputs can only have 0 or 1 values.

Quantum Cost: Quantum cost refers to the circuit implementation cost in terms of its primitive gates in quantum computing. In the reversible binary circuit, the quantum cost is the number of elementary 1-qubit and 2-qubit quantum logic gates such as NOT, Controlled-V, Controlled-V+, and CNOT. The quantum cost, attributed to each of these gates, is one [24]. Similar to reversible binary circuit, the quantum cost of reversible ternary circuit is the number of primitive gates including 1-qutrit shift gates and 2-qutrit M-S gates. The quantum cost of each of these gates is one [11].

2.2. Basic reversible ternary gates

In this section, the shift and M-S gates functions used for designing reversible ternary circuits in section 4 are explained.

2.2.1. Reversible ternary shift gates

In this subsection, we present the basic gates in reversible ternary circuits. There are six 1×1 shift gates for 3! Permutations of 0, 1 and 2, which are elementary gates with the quantum cost of one [11]. Table 1 shows operations of the permutative gates. This is known as a Z-transformation and the symbol in quantum circuits is shown in Fig. 1.

2.2.2. Reversible ternary Muthukrishnan-Stroud gates (M-S gates)

Muthukrishnan and Stroud proposed a primitive 2-qutrit quantum gate which can be implemented using ion-trap technology [14]. Fig. 2 shows the symbol of M-S gate. In Fig. 2, A is the control input and B is the target input, Q is the Z-transformation (where Z = +1, +2, 01, 02, 12) of the input B whenever A = 2, otherwise Q = B. The quantum cost attributed to this gate is one [11]. The complexity or quantum cost for a reversible ternary circuit refers to the number of M-S gates and shift gates which are used to realize the given circuit.

3. Introducing the ternary coded decimal codes

In this section, firstly we explain TCD codes; and then, in the following subsection, we explain that how two one-digit decimal numbers are