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Exploring N^{3}ASIC technology for microwave imaging architectures

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ABSTRACT

When studying a new technology a critical issue is to understand its performance with respect to CMOS circuits. In this work, we analyze the performance of Nanoscale Application Specific Integrated Circuits (NASIC) and its CMOS-friendly implementation, the N^{3}ASIC. We have created a circuit model using VHDL language. The model includes the estimation of area and power consumption of devices and blocks that can be hierarchically connected to form complex circuits. Using this model we designed a hardware accelerator for an image reconstruction algorithm for biomedical application. We synthesized the same architecture with a 45 nm-CMOS and a 7-nm FinFet library to make a comparison. The results obtained for the N^{3}ASIC are very interesting, showing a substantial reduction in both circuit power and area.

1. Introduction

The scaling process of MOSFET devices has driven the extraordinary evolution of modern computational systems. Unfortunately it is reaching its limits [1]. For many researchers the main goal is therefore to find innovative ways to further improve computational systems used in more demanding applications. One possibility is to study and design devices that have a totally different behavior from transistors. Examples are the Molecular Quantum Dot Cellular Automata [2,3] or the Nanomagnet Logic [4–6] technologies. Here, the information is no more represented by using a current or a voltage, but by a charge or magnetic configuration. The opposite approach to improve computational systems can be exploited by designing unconventional architectures. These new architectures tries to overcome the limitations of traditional Von-Neumann based architectures. An example of this approach is represented by the so-called Logic-In-Memory principle [7–9], where logic computation and information storage are performed at the same level, greatly enhancing the overall performance of the circuit. There is however a third possibility to overcome the limitations of current computational systems. It is based on the idea of applying the same architectural principles normally applied at gate-level with MOSFET technology, but at nanoscale level using new devices.

This is indeed the solution used by Nanoscale Application Specific Integrated Circuits (NASIC) technology [10]. Despite having a name similar to ASIC circuits, the two technologies are quite different. In NASIC technology circuits are represented by nanoscale Programmable Logic Array (PLA) [11], while in standard ASIC, circuits can be made by a combination of any kind of logic circuits. A PLA is composed by regular arrays of logic gates divided in two planes, one composed by AND logic gates and the other composed by OR logic gates. The combination of these two planes makes it possible to design any kind of logic functions. NASIC technology applies this concept at transistor level using at the same time new devices. The structure of the circuits is based on a grid of silicon nanowires. At the junction of these nanowires, depending on the logic function that should be implemented, a gate-all-around silicon nanowire transistor can be fabricated or not. The technology has undergone two major improvements, one called N^{3}ASIC [12] and the other one called SkyBridge [13]. In both these implementations the concept of NASIC was elevated to a new level by exploiting the possibilities offered by 3D fabrication processes. More details on the technology are provided in Section 2.

The possibilities offered by NASIC technology, in all its implementations, are huge. To understand them it is necessary to design and analyze a complex and realistic circuit. Parameters like area occupations and power consumption can be estimated only at architectural level. This is exactly what we have done in this work. The goal was to analyze the effectiveness of this new technology in comparison with state of the art CMOS technology. For this purpose, we selected a complex architecture to be used as a case of study. The chosen architecture is a hardware accelerator for the Microwave Imaging via Space Time (MIST) beamforming algorithm [14]. This is an algorithm used in image reconstruction techniques for biomedical applications [15]. It must be accelerated to be used in real-time measurements [16]. Details on the algorithm can be found in Section 2. The circuit was chosen for two reasons. First it is a realistic circuit, as it is currently employed in microwave imaging systems [17]. Secondly it was selected because

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hardware accelerators are an ideal application for this new technology.

Our goal was to perform a worst-case analysis of N^{3}ASIC technology. The analysis is performed in a worst-case scenario because we do not have enough data to perform a more accurate modeling. With the data available in literature there was only the possibility to develop a model able to estimate the performance in the worst-case. Furthermore, given that both NASIC circuits based on Silicon Nanowire FETs and SkyBridge technology theoretically offer better performance, the results obtained in this work represent the worst-case performance that can be obtained with this technology. As will be clear from Section 5, the obtained results highlights better performance than state of the art MOSFET circuits also in this case. As a consequence, with further technological improvements, performance can only be better. The N^{3}ASIC technology is described by using a VHDL model, which is able to simulate not only the behavior of the technology but also to evaluate area and power consumption of circuits. Section 4 describes the model and the implementation of the architectures using N^{3}ASIC technology.

To summarize, this work as several major contributions.

- We developed a new RTL model written in VHDL language for this technology. It allows us to easily design and simulate N^{3}ASIC circuits, evaluating at the same time area occupation and power consumption.
- By using both existing and custom-developed tools and the our RTL model, we designed and analyzed a complex and realistic circuit based on N^{3}ASIC technology.
- We compared the performance with MOSFET circuits, performing a synthesis of the same architecture with a 45 nm technology node and a 7 nm FinFet predictive technology node [18], demonstrating that the N^{3}ASIC version has lower area and power consumption.

2. Background

2.1. Technological background

Different kinds of nanoarray structures have been proposed in literature. All solutions are based on a set of perpendicular nanowires, organized in matrices and conceptually similar to PLAs. A certain number of configurations are currently under investigation, such as nanoPLA, CMOL [19] and NASIC, introduced in Refs. [11,20] and extended in Ref. [21]. Nanoarray based circuits have a typical crossbar structure. Semiconductor nanowires are organized in a 2D grid and transistors are fabricated at some cross points. The position of these active elements, which can be xnwFET [11] or gate all around transistors (GAA) [22], determines the logic function implemented by the circuit. Circuits are organized in tiles (Fig. 1A). Complex architectures are composed by an array of tiles interconnected to each other.

A dynamic logic control scheme is used in order to correctly propagate signals through the circuit. Considering Fig. 1A, two logic planes can be identified, the former is named *NAND1* and the latter *NAND2*. The dynamic behavior is obtained with a couple of precharge and evaluation signals: *hpre*, *heva*, *vpre*, *veva* (Fig. 1C). These control signals, generated by CMOS circuitry, guarantee the correct information propagation within a tile. From a practical point of view, the first two signals, (*hpre* and *heva*), propagate information from the inputs to the outputs of the *NAND1* logic plane. The other two, (*veva* and *vpre*), control the transmission towards the tile outputs through the *NAND2* plane. Signals are implicitly latched on the nanowires themselves. On the tile periphery, microwires carry the power supply signals V_{dd} and V_{ss}.

Despite their promising characteristics in terms of device density and low power consumption, NASIC technology suffers from a non-negligible defect rate during the manufacturing process [23,24]. In literature, different fault tolerance techniques have been proposed. One of them implies the use of FaTToR algorithm [25]. This algorithm increases circuit fault tolerance changing transistor disposition without area overhead. Other algorithms use instead hardware redundancy combined with biasing voting techniques [26,27].

Nanoarray have another important limitations. Due to the planar nature of this technology, logic and interconnection wires lie on the same plane. Routing of logic signals is very inefficient leading to a huge wasted area. This problem has been addressed on a recently proposed structure, named N^{3}ASIC, that is based on a hybrid 3D nanoscale CMOS fabric [28]. This fabrication process enables full integration with CMOS technology, as reported in Ref. [12]. A single unconventional manufacturing step is needed at the beginning of the fabrication process, then standard lithographic steps are used. The general circuit organization recalls the structure of a NASIC tile. As depicted in Fig. 1B, the two logic planes *NAND1* and *NAND2* are no longer placed on the nanowire grid, but they are separated in two sub-circuits. The 3D structure has been further exploited in the so-called SkyBridge solution [13,29]. This innovative solution uses a 3D fabrication process not only to house interconnection wires, but also for logic computation [30], greatly enhancing circuits density.

The building blocks of a N^{3}ASIC circuit are semiconductor nanowires. These structures can be fabricated using techniques such as nanoimprinting, block copolymer assembly or patterning (Fig. 2A) [28,31]. Nanowires are generally built on a standard ultra-thin Silicon on Insulator (SOI) wafer. As happens with NASIC, the position where transistors are fabricated (Fig. 2B) defines the logic function implemented by the circuit. Input signals are carried through the circuit towards the proper metal gate, with orthogonal metal 1 (M1) lines (Fig. 2C). The same technique is applied to output signals. Interconnections among logic planes and different tiles is obtained with metal wires, located on additional layers. The information propagation is obtained by using the same dynamic logic scheme used for a normal NASIC circuit. The final structure of a single AND gate is depicted in Fig. 1B. Since CMOS integration is required, a greater space is needed between nanowires with respect to 2D NASIC. For this reason, the higher density of NASIC technology (33× a standard CMOS design), is reduced to 3× in N^{3}ASIC [32], but the routing of interconnection signals is greatly improved.

2.2. Ultra wide band screening system

The aim of an Ultra-Wideband (UWB) screening system for breast cancer detection is to detect cancer tissue by using UWB electromagnetic pulses [15]. It is not an invasive solution for the breast, and it has an accuracy that is comparable to the mammography. This technique measures the difference of the dielectric constant of a tumor with respect to the other breast tissues. The breast is irradiated with an array of antennas, each of them transmitting short pulses in the frequency range from 0.5 GHz to 10 GHz. Each pulse is then backscattered by the breast tissues based on their dielectric constant. The dielectric constant is 80 times higher in cancer tissue with respect to a fatty tissue. The cancerous tissue reflects, as a consequence, more UWB pulses than normal tissue. The backscattered signals are collected and processed in order to reconstruct the breast image (2D or 3D).

Fig. 3 depicts the block diagram of the UWB system. In this configuration, named *monostatic*, antennas are used both as transmitters and receivers. Each of them is connected to a dedicated transceiver that sample the incoming backscattered UWB signals. The antenna array scans the breast and communicates with front-end electronics. The front-end sends the received signals to the image unit. The front-end interface pre-process samples and stores them into a memory. When a complete scan of the breast if performed, all samples are read from the memory and processed by the imaging unit. It computes and generates a map of the reflected energy values related to each breast volume location, named *voxel* or volume pixel. The final resolution of the image strictly depends on the total number of *voxel*. It is worth noticing that a complete scan of the breast can be performed in a short time, typically less then a second [33]. On the contrary, the computation of the