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50–830 MHz noise and distortion canceling CMOS low noise amplifier

Sana Arshad[a,*], Rashad Ramzan[b], Qamar-ul Wahab[c]

[a] Electronic Design Centre, Department of Electronic Engineering, NED University of Engineering and Technology, P.O. Box 75270, Karachi, Pakistan
[b] Electrical Engineering Department, United Arab Emirates University, P.O. Box 15551, Al-Ain, UAE
[c] IFM Department, Linkoping University, Sweden

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ABSTRACT

In this paper, a modified resistive shunt feedback topology is proposed that performs noise cancelation and serves as an opposite polarity non-linearity generator to cancel the distortion produced by the main stage. The proposed topology has a bandwidth similar to a resistive shunt feedback LNA, but with a superior noise figure (NF) and linearity. The proposed wideband LNA is fabricated in 130 nm CMOS technology and occupies an area of 0.5 mm^2. Measured results depict 3-dB bandwidth from 50 to 830 MHz. The measured gain and NF at 420 MHz are 17 dB and 2.2 dB, respectively. The high value of the 1/f noise is one of the key problems in low-frequency CMOS designs. The proposed topology also addresses this challenge and a low NF is attained at low frequencies. Measured S11 and S22 are better than −8.9 dB and −8.5 dB, respectively within the 0.05–1 GHz band. The 1-dB compression point is −11.5 dBm at 700 MHz, while the IIP3 is −6.3 dBm. The forward core consumes 14 mW from a 1.8 V supply. This LNA is suitable for VHF and UHF SDR communication receivers.

1. Introduction

The shrinking CMOS technology has revealed wideband LNAs as promising contenders for accommodating multiple frequency bands in a single unit. In the available wideband topologies, the Distributed Amplifier (DA) [1–3], the Common-Gate (CG) Amplifier [4–11] and the Resistive Shunt Feedback Amplifier [12–15], pose intrinsic broadband behavior [16]. Although the DAs offer a wideband characteristic, the additive distribution of the gain over several stages lead to a high power consumption and inhibit their use in low-power applications. Wideband input impedance in a CG amplifier can be obtained with the aid of one inductor that neutralizes the gate-to-source capacitance C_{gs} of the transistor. However, the transconductance of the transistor is defined by the input matching criteria, which limits the gain and noise response. The resistive shunt feedback LNAs have broadband response in combination with a Common Source (CS) amplifier, which itself is intrinsically narrowband in nature [12–15]. The input impedance for this topology depends primarily on the feedback resistor, along with the loop gain of the amplifier [12]. For wide bandwidth, the feedback resistor should be small, which on the other hand degrades the NF. Hence it can be inferred that, broadband behavior of the CG and resistive shunt feedback LNAs is limited due to their poor noise response. Positive/ negative feedback [17–19] and noise-canceling [4–6] techniques are employed to break the correlation between the noise figure, gain and input matching in CG LNAs. In resistive shunt feedback LNAs, series or shunt peaking aids in enhancing the bandwidth, while a large feedback resistor is used to attain a good NF [20].

In this paper, a modified resistive shunt feedback topology is proposed that can deliver optimal bandwidth, NF and gain concurrently without series or shunt peaking. It essentially performs noise and distortion cancelation to achieve the said goals. The proposed LNA depicts measured bandwidth between 50–830 MHz. This LNA can be utilized in multistandard front-ends for VHF and UHF bands. The noise-cancelation feature in the proposed LNA helps to reduce the low-frequency 1/f noise and makes the FETs feasible for low frequency applications, which are classically reserved for BJTs [21]. In general, the 1/f noise of FETs is several orders of magnitude greater compared to the noise at high frequency.

The paper is structured as follows. In Section 2, the theory of proposed LNA including detailed derivations of input impedance, noise and distortion cancelation are presented. The LNA component values are listed in Section 3, while fabrication and measurement results are illustrated in Section 4. Section 5 concludes the paper.

* Corresponding author. Present Address: Electronic Design Centre, Department of Electronic Engineering, NED University of Engineering and Technology, Karachi, P.O. Box 75270, Pakistan.
E-mail addresses: sana@neduet.edu.pk (S. Arshad), rashad.ramzan@uaeu.ac.ae (R. Ramzan), wahab.qu@gmail.com (Q.-u. Wahab).

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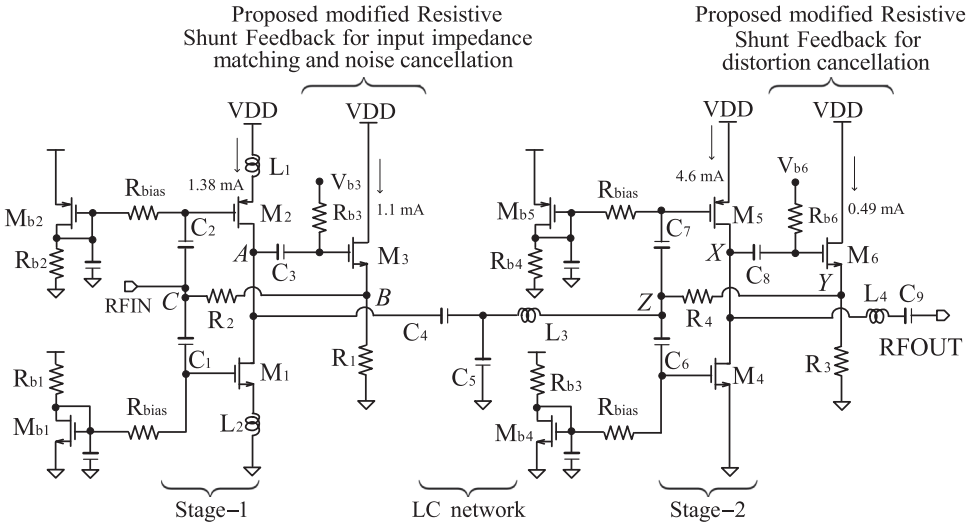

Fig. 1. Proposed single ended two stage wideband LNA employing modified resistive shunt feedback for input impedance matching and noise cancelation in stage-1 and distortion cancellation in stage-2. All the transistors have length of 130 nm and width given as M_1 = 130 μm, M_2 = 420 μm, M_3 = 30 μm, M_4 = 70 μm, M_5 = 130 μm and M_6 = 90 μm. The resistors are R_1 = 1 kΩ, R_2 = 212 Ω, R3 = 120 Ω, R_4 = 270 Ω while other components are L_1 = 772 pH, L_2 = 683 pH, L_3 = 4.99 nH, L_4 = 2.62 nH, C_1 = 15 pF, C_2 = 15 pF, C_3 = 9.3 pF, C_4 = 12 pF, C_5 = 800 fF, C_6 = 1.9 pF, C_7 = 1.9 pF, C_8 = 13 pF, C_9 = 11 pF.

2. LNA circuit theory

2.1. Architecture

Fig. 1 shows the proposed two stage wideband LNA with the proposed feedback. In stage-1, the proposed feedback reduces the noise generated by various components, besides relaxing the input matching criteria, while it enhances the linearity, in stage-2.

The transistors M_1-M_2 in stage-1 and M_4-M_5 in stage-2 are placed in an inverter type current-reuse fashion to achieve a high gain with reduced power consumption. The capacitors C_1 and C_2 couple RF input to the gates of M_1-M_2 and towards the source of M_3 via resistor R_2. The capacitor C_3 carries output of stage-1 to the proposed feedback network, which consists of a Source follower M_3 with resistances R_1 and R_2 where R_1 serves as the load for M_3. The inductors L_1 and L_2 enhance the input matching at high frequency, while at low frequency the impedance matching is mainly provided by the feedback network of stage-1. DC blocking capacitor C_4 isolates the bias voltages of stage-1 and stage-2. In combination with C_5 and L_3, it maintains LNA gain in central region of the simulated passband.

In stage-2, C_6 and C_7 deliver output of stage-1 to the gates of M_4-M_5, respectively. The source follower M_6 produces distortion in accordance with the distortion it samples from the output node of M_4-M_5. The output of M_6 is carried by R_4 to the gates of M_4-M_5. The difference of the actual input signal and the scaled non-linear feedback signal enhances the linearity as discussed in detail in Section 2.4. The capacitor C_9, inductor L_4 and the output impedance of stage-2 collectively generate the 50 Ω output matching for chip measurement without any additional buffer.

2.2. Input Impedance

Fig. 2(a) presents the low-frequency small signal model of the proposed LNA, while the small signal model of feedback part of stage-1 is also drawn separately in Fig. 2(b) for input impedance analysis at low frequency. Due to the addition of the feedback network, the input impedance depends both on the impedance looking into the gates of M_1/ M_2 and on the impedance looking into the source of M_3 (Fig. 1). At low frequency, the transistors M_1 and M_2 would offer an infinite impedance at the input (gate) node leaving only the feedback path for input impedance matching. Hence, the small signal model of the feedback network of stage-1 is referred from Fig. 2(b), where a test voltage source V_t with current i_t is applied at the input. KCL at node *B* leads to Eq. (1)

$$i_t + g_{m3}V_{gs3} = \frac{V_t - i_t R_2}{R_1} \tag{1}$$

where V_{gs3} is the gate-to-source voltage of M_3 and can be approximated as $V_a - V_t + i_t R_2$. Here V_a is the voltage at node *A* as per Fig. 1 and g_{m3} is the transconductance of M_3. Using Eq. (1), the low-frequency input impedance ($Z_{in,lf}$) for the proposed LNA is given by Eq. (2).

$$Z_{in,lf} = \frac{R_1 + R_2(1+g_{m3}R_1)}{1+g_{m3}R_1(1-A_1)} \tag{2}$$

Where A_1 is the gain of the forward path of stage-1. In comparison with the resistive shunt feedback topology, which has an input impedance equal to $R_F/1+|A_{RSF}|$ (with R_F, A_{RSF} be the feedback resistor and loop

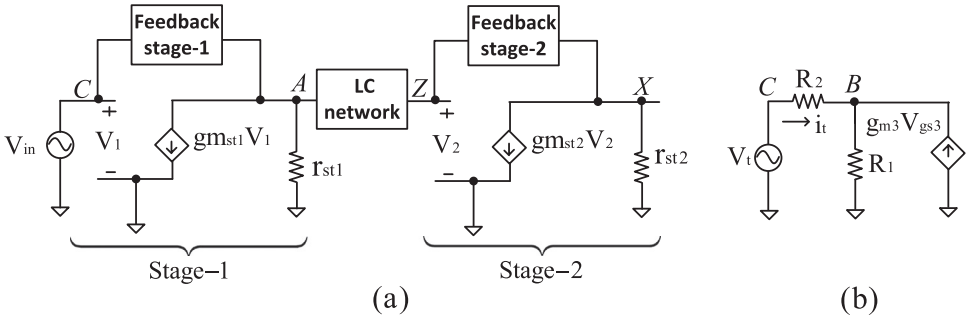

Fig. 2. (a) Simplified low frequency small signal model of the proposed LNA (b) Small signal model of feedback part of stage-1 drawn individually to find its impedance for input matching. Test voltage source Vt is applied for input impedance calculation.