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Recent advances in EM and BTI induced reliability modeling, analysis and optimization (invited)☆

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ABSTRACT

In this article, we will present recent advances in reliability effects such as electromigration on interconnects and Negative/Positive Bias Temperature Instability (N/P BTI) effects on CMOS devices, which are the most important reliability concerns for VLSI systems specifically at the nanometer regime. We will start with the grand reliability challenges facing the semi-conductor and computing industry. Then, we will first present recent advances in the electromigration (EM) modeling and assessment techniques at the circuit level, the full-chip level and the system level. We will focus on the recently proposed advanced EM modeling techniques including stress-oriented physic-based EM models, EM modeling considering the time-varying temperature and current density changes, EM recovery effect modeling, the more general physics-based 3-phase EM models and the finite-difference-method based numerical analysis technique for dynamic EM stress analysis. Then we will present recent developments for dynamic reliability management at the system level, where EM-induced lifetime and performance can be traded off and the EM recovery effects can be leveraged for a longer lifetime on different computing platforms.

For BTI effects, we will briefly explain the key mechanisms behind it first. Then, we will demonstrate how to bring *aging-awareness* to EDA tool flows based on our so-called degradation-aware cell libraries. Afterwards, we will present the impact of BTI effects on the leakage and dynamic power showing that BTI impact not only affects circuits' delay over time (as in the traditional view), but also the overall power of circuits. Towards removing guard-bands and hence increase the efficiency, we will present how aging-induced stochastic timing errors can be translated into deterministic and controlled approximations in which aging effects are suppressed with a minimum loss in quality. Finally, we will demonstrate *short-term aging effect* which is a recent discovery that is hardly explored until now. In fact, *short-term* aging effects are a paradigm shift in BTI from sole long-term reliability degradation, which is observable in the order of months and years as in the traditional view, to an emerging reliability degradation, which is observable in a significantly smaller time domain in the order of milliseconds and even microseconds. Some of the developed EM models and assessment programs can be downloaded at https://github.com/sheldonucr/physics_based_em_assessment_analysis. The developed aging models, degradation-aware cell libraries, reliability framework, etc. are publicly available at: http://ces.itec.kit.edu/dependable-hardware.php. They are ready to be directly used with existing EDA tool flows like Synopsys without requiring any modifications.

1. Introduction

Reliability has become a major design challenge and limiting factor for nanometer VLSI designs due to the high failure rates in deep submicron and nanoscale devices. It is expected that the future chips would show signs of reliability-induced aging much faster than previous generations. Among many reliability effects, the most concerning are electromigration (EM) in interconnects and Bias Temperature Instability (BTI) for CMOS devices as a result of increasing power density and aggressive transistor scaling. In fact, as technology nodes were being reduced to below 45 nm, the quality of the gate dielectric became severely less leading to higher leakage currents due to tunneling. To overcome this problem, manufacturers like Intel replaced silicon dioxide with the so-called "high-k material"

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which is a new kind of materials composition that gives a higher dielectric constant [1]. However, the susceptibility of transistors to strain/stress in such new materials (e.g., HfO_2) is higher than the older materials (e.g., SiO_2) [2,3]. For instance, measurements [2] demonstrated that the using the new high-k material results in higher degradation with respect to Positive Bias Temperature Instability (PBTI) and a similar degradation with respect to Negative Bias Temperature Instability (NBTI). As a result, scaling in conjunction with high-K materials has made aging phenomena that have often been assumed to be negligible become noticeable.

Electromigration failure of interconnects has been a long-standing concern for the development of highly reliable VLSI systems. Despite intense efforts from both industry and academia following the first observation of EM-related failure of Al circuit interconnects by James Black [4], it has proven impossible to find a robust process solution by material modification for either Al or the more recently introduced Cu metal system. EM failure can only partially be mitigated with process solutions and ultimately needs to be controlled and managed at circuits and even system levels in a cross-layer a fashion. The International Technology Roadmap for Semiconductors (ITRS 2014) predicts that the lifetime of wires due to EM will decrease by half for each new generation as shown in Fig. 1, which shows the actual and predicted lifetime scaling versus interconnect geometry [5]. It has been predicted that EM failure will become more significant for interconnects in FinFET based technologies at 10 nm and it is urgent to address this "EM crisis" which has recently prompted intense efforts to develop more robust interconnect materials, structures and design solutions [6,7].

Traditional compact EM checking approaches such as Black's equation [4] and Blech product [8] can lead to significant over-design [9]. These conservative design rules are not suitable for future technology scaling since more design guard bands are required for chip timing accuracy, and thus such a worst-case design methodology results in inefficiency and considerable penalties in the area, performance, power, and reliability budgets. Therefore, during the design process, a balance must be found to ensure circuit performance without seriously impairing electromigration reliability. Achieving this balance requires a thorough fundamental understanding of EM physics kinetics and the dominant factors for the failure process.

In this article, we review some of the recent advances in EM modeling and cross-layer EM-induced dynamic reliability management techniques and recent BTI modeling and optimization techniques. The review article does not intend to cover all the recent development for the EM and BTI related topics. The topics not covered in this article does not diminish their contributions and values to the communities.

The article is organized into two major sections: Section 2 for EM related modeling, analysis and optimization and Section 3 presents the BTI impacts on circuits.

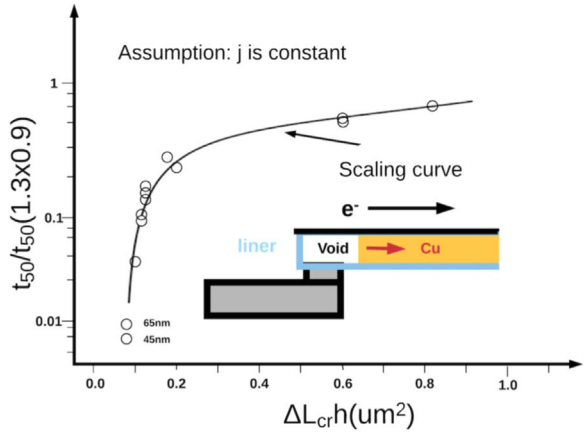

Fig. 1. The lifetime of interconnect wires versus technology nodes by ITRS2014.

Specifically, for the first EM Sections 2, 2.1 reviews the classic EM physics and existing EM failure models and discusses limitations of those models. Section 2.2 reviews the mainstream stress-based modeling of EM failure kinetics and the important Korhonen's equation. It further presents the physics-based EM models and recently proposed physics-based compact EM models and more accurate physics-based three-phase EM model. Section 2.3 present the recently proposed compact two-phase EM models and the more general three-phase EM models, which can better describe the wire EM-induced resistance changes over time. Section 2.4 introduces the dynamic EM model to consider transient stress evolution when the wires are stressed under time-varying current flows and the EM recovery effects. We also present a parameterized new equivalent DC current based EM model to consider the recovery and transient effects. Section 2.5 gives the closed form expressions (for the Korhonen's equation) for stress evolution over time for some commonly seen multi-segment wires based on Laplace transformation method. Section 2.6 introduce another closed form solutions to the Korhonen's equation for stress developments of multi-segment wires in a straight line using the integral transformation method. Section 2.7 presents the new voltage-based steady-state EM-induced stress analysis and new EM immortality check method for general interconnect trees. Section 2.8 presents the recently developed finite difference based analysis technique for Korhonen's equations. Section 2.9 shows the recently developed EM-induced dynamic reliability management and energy or lifetime optimization techniques for many-core dark silicon microprocessors and datacenters.

For the second BTI Section 3, we start in Section 3.1 by explaining briefly the key mechanisms at the physical level behind aging phenomena. Then, in Section 3.2 we demonstrate the impact of aging-induced degradation on the performance and power of circuits. Afterwards, we show in Section 3.3 the ultimate impact of aging effects at the system level. We also show how approximate computing principles can be applied to translate stochastic aging-induced timing errors into deterministic and controlled approximations. In Section 3.4 we show how BTI effects in conjunction with voltage scaling can result in short-term reliability degradation leading to transient errors akin to the temporal violation of aging guardbands at the moment of voltage switch. Finally, Section 4 concludes the article.

2. Electromigration (EM) modeling, analysis and optimization

2.1. Electromigration fundamentals

Electromigration (EM) is a physical phenomenon of the oriented migration of metal (Cu) atoms along a direction of applied electrical field due to the momentum exchange between atoms and the conducting electrons. Atoms (either lattice atoms or impurities) migrate toward the anode end of the metal wire along the trajectory of conducting electrons. This oriented atomic flow results in metal density depletion at the cathode, and a corresponding metal accumulation at the anode end of the metal wire. This depletion and accumulation happen because atoms cannot easily escape the metal volume as the metal wires are confined by the so-called diffusion barriers. A Cu damascene interconnect wire typically is confined or embedded by metallic barriers such as Ta and capped with either a dielectric (such as SiN) or a metallic layer (CoWP) as shown in Fig. 2.

As a result, the wire volume changes, which is induced by the atom depletion and accumulation due to migration leading to build-up of hydrostatic stresses across the conductor resulting in tension at the cathode end and compression at the anode end of the wire [10–12]. Over time, the continuous unidirectional current flow increases these stresses, as well as the stress gradient along the metal line. The stress gradient actually serves as the back-force to reduce the EM-induced metal migration flow. In some cases, usually when a wire is long or

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