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A novel design for ultra-low power pulse-triggered D-Flip-Flop with optimized leakage power

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ABSTRACT

The power efficiency and reducing the layout area are two main concerns in D-Flip-Flops (D-FF) design. In this paper, a novel architecture is presented for the pulse-triggered D-FF in the CMOS 90-nm technology. This novel architecture utilizes a transmission gate to control the input data and the leakage power. The Pulse Generator (PG) is also modified to reduce the number of required transistors and the clock pulse delay. In addition, the pull-up P-MOS transistor is controlled by input data to reduce the power dissipation. The proposed D-FF is simulated using Hspice. The simulation results show that the proposed architecture has improvement in terms of power consumption, D-to-Q delay, and Power Delay Performance (PDP) in comparison with other D-Flip-Flop architectures.

1. Introduction

One of the most important concerns in today's electronics is the device power efficiency [1,2]. This issue becomes more important when facing integrated circuits [3]. The memory cells and microprocessors are not exempt from this issue. One of the basic elements used for storage purposes is Flip-Flops (FFs) [4,5]. The wide use of FFs in pipelining techniques shows the importance of this device's power efficiency [6,7]. There are three main groups of Flip-Flops: 1) Pulse Triggered-Flip-Flops (PT-FFs), 2) Transmission Gate-Flip-Flops (TG-FFs) and 3) Master Slave-Flip-Flops (MS-FFs) [8–12].

PT-FFs are more commonly used due to their single-latch architecture, speed advantage, and their low power consumption [13]. The PT-FFs are divided into two groups based on the place of pulse generator: 1) implicit PT-FFs, in which the latch contains the pulse generator, and 2) explicit PT-FFs, in which the latch is separated from the pulse generator [14]. The explicit PT-FFs are more efficient in case of power, but their speed is lower than implicit PT-FFs [15]. Here, we have chosen explicit PT-FF and optimized its properties.

In the PT-FFs, the triggering pulse is used to trigger the latch. This simple one latch architecture would result in a simpler circuit and lowers power consumption in comparison with the MS-FFs [15]. Although PT-FFs seem to be the best choice for our purposes, but the pulse width must be considered delicately. The authors of [11–29] proposed different PT-FF designs that have improved the Flip-Flops performance. The main problem with all of these designs occurs in case of changing the value of output from “0” to “1”. It is the direct result of their complex architectures [26]. It is because in all of these Flip-Flops when the output is transiting from “0” to “1”, the input signal must pass through at least 2 or 3 transistors, which means 2 or 3 transistors delay, so the D to Q delay performance would face a huge delay time [29]. In this paper, this delay time is reduced as much as possible. These architectures and their problems will be discussed in Section 2.1 more thoroughly.

In this paper, a new design methodology is proposed for PT-FFs to optimize the power consumption, layout area, and “0” to “1” latching delay. This design controls the input data by the transmission gate. The utilized Pulse Generator (PG) reduces the complexity of the FF, and optimizes the power efficiency of this novel D-FF. This novel architecture contains a signal feed-through scheme, which is controlled by an N-MOS transistor. The proposed architecture is simulated in Hspice. The results show that the proposed D-FF architecture has improvements in terms of Power Delay Performances (PDPs) in comparison with other D-FF architecture.

This paper is organized as follows: the proposed approach with its background is discussed in Section 2. In Section 3 the proposed architecture is simulated and its features are compared with similar designs and finally, Section 4 concludes this paper.

2. Approach

2.1. Conventional PT-FF architecture

The block diagram of several Flip-Flops is shown in Figs. 1–6. Each of them has some unique advantages and disadvantages. Fig. 1 shows a

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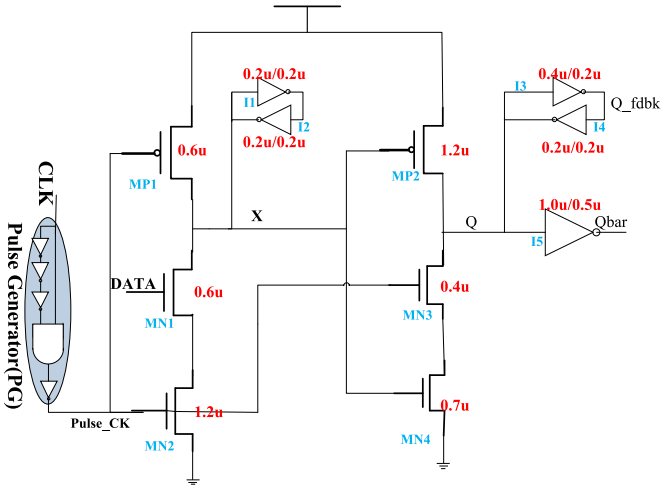

Fig. 1. The utilized ep-DCO Flip-Flop architecture in [11].

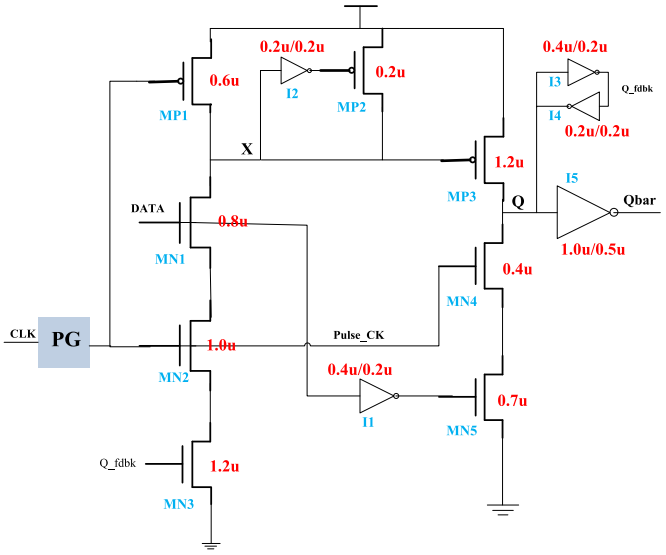

Fig. 2. The utilized CDFF architecture in [20].

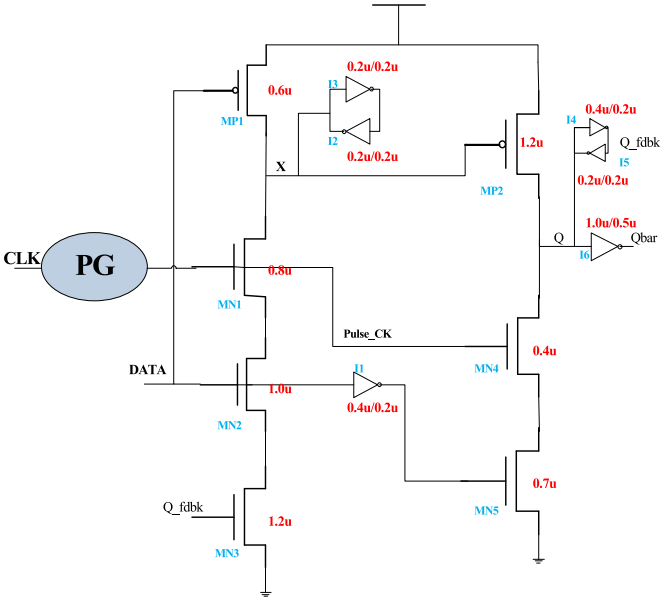

Fig. 3. The utilized SCDFF architecture [21].

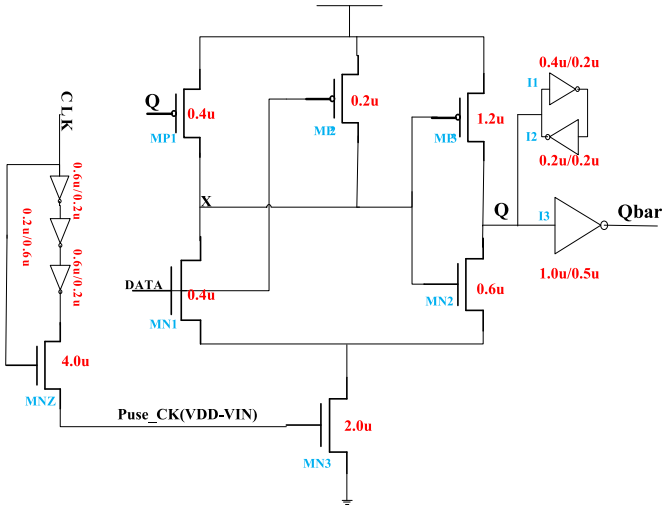

Fig. 4. The utilized MHLFF architecture in [23].

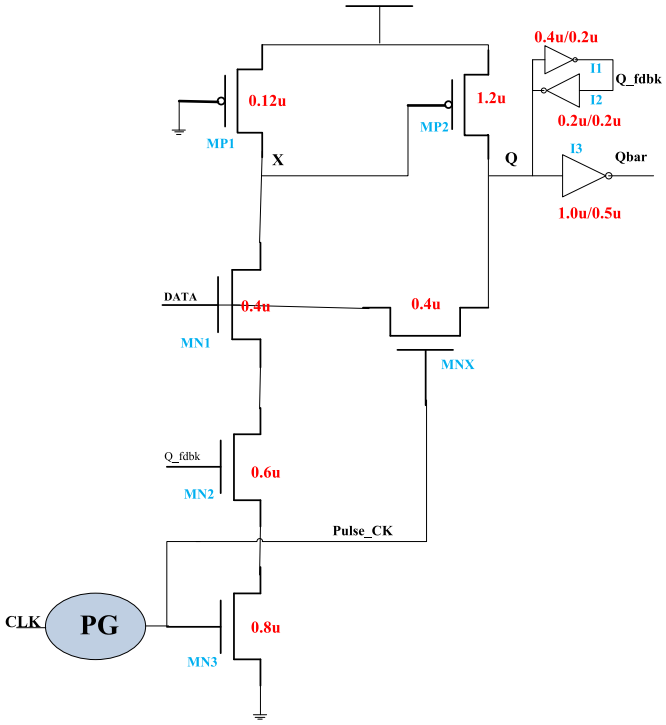

Fig. 5. The utilized pulse-triggered flip-flop with a feed through technique in [26].

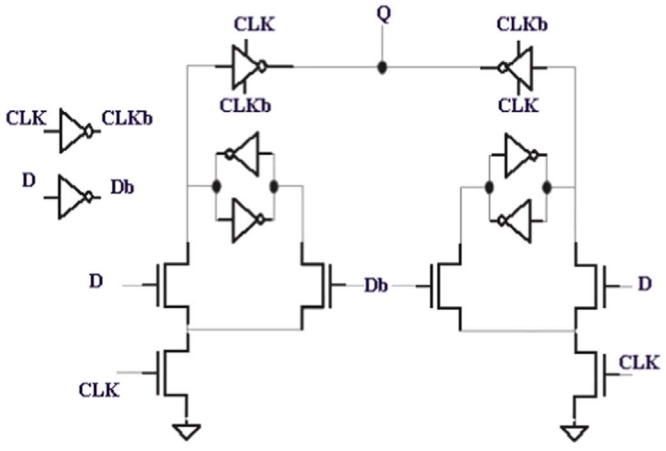

Fig. 6. The utilized dual-edge-triggered Flip-Flop architecture in [33].