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A new low-power dynamic circuit for wide fan-in gates

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ABSTRACT

In this paper, a new dynamic circuit is proposed to reduce the power consumption of wide fan-in gates. Since the voltage difference across the pull-down network determines the output in the proposed circuit, the voltage swing on the pull-down network can be lowered to decrease the dramatically increasing power consumption of wide fan-in gates. Wide fan-in OR gates are designed and simulated using the proposed domino circuit in 90 nm CMOS technology. Simulation results exhibit up to 2.62X improvement in noise immunity and 44% reduction in power consumption compared to the conventional domino circuits at the same delay. Moreover, a 2-read, 1-write ported 64-word × 32-bit/word register file is designed using the proposed domino circuit. The Register file is simulated using low-Vth 90 nm CMOS model in all process corners. The results shows 25% power reduction and 32% speed improvement for the proposed register file in comparison with the conventional register file at the same noise margin floor.

1. Introduction

Wide fan-in gates have many applications in critical and high performance units of microprocessors such as multi-ported register files [1]. To implement these gates in CMOS, dynamic circuits have been extensively used because of their higher speed and smaller chip area compared to the static counterparts. However, dynamic circuits suffer from some drawbacks including higher power consumption and lower noise immunity [2]. Nowadays, power consumption has become one of the most important concerns for integrated circuit designers especially with the rapid growth in portable devices. To reduce the power consumption, the supply voltage is scaled down with technology scaling. Moreover, as technology is scaled down, the threshold voltage (Vth) must be reduced to achieve a high performance, which results in an exponential increase in subthreshold leakage current due to the exponential dependence of off-current to Vth [3]. Consequently, leakage power increases which leads to a lower noise immunity, especially for wide fan-in gates. By increasing the fan-in in dynamic gates, the power consumption increases due to the larger switching capacitance and the noise immunity will reduce due to a larger number of parallel branches in the pull-down network. Therefore, according to applications of wide fan-in dynamic gates, reducing the power consumption while improving the noise immunity is necessary for high-speed processors.

1.1. Related works

A most widely used dynamic circuit is the domino circuit, which is shown in Fig. 1. Several derivatives of domino circuit are reported in the literature to address the above-mentioned issues. These circuit techniques can be classified into two groups. First is the ones propose new keeper circuitry such as high speed domino (HSD) [4], conditional keeper domino (CKD) [5] and leakage current replica (LCR) keeper domino [6], as shown in Fig. 2(a)-(c), respectively. On the other hand, the second group reconstruct the evaluation network such as diode-footed domino (DFD) [7], current comparison based domino (CCD) [8] and voltage comparison based domino (VCD) [9] as shown in Fig. 2(d)-(f), respectively. However, although these circuit techniques improve some design parameters, they degrade other parameters. For example, decreasing the power consumption generally results in degradation of the noise immunity or performance.

1.2. Paper overview

Our work falls into the second group, and targets reducing the power consumption. To reduce the power consumption, all effective components, i.e. switching (dynamic), leakage (static) and short circuit power consumption need to be reduced. In more scaled technologies, a large portion of the total power consumption attributed to the leakage current, thus reducing the leakage power becomes more crucial

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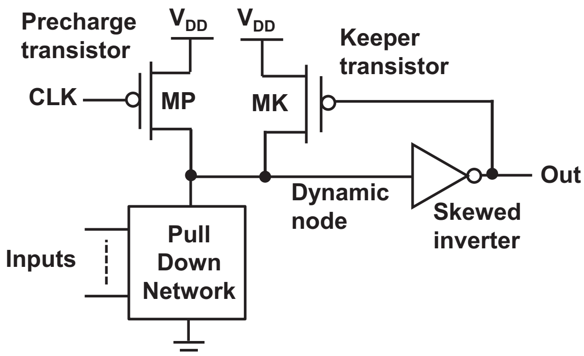

Fig. 1. Conventional domino circuit.

especially for wide fan-in gates. In the proposed domino circuit, the total power consumption is reduced by lowering the voltage swing across the pull-down network and reducing the subthreshold leakage current. Furthermore, the proposed circuit technique improves the noise immunity. To demonstrate the efficiency of the proposed circuit, a 64-word × 32-bit 2-read, 1-write ported register file is designed using the proposed circuit technique.

The rest of the paper is organized as follows. The proposed domino circuit is explained in Section 2. Simulation results and comparisons are given in Section 3. Implementation and simulation of a register file designed using the proposed circuit will be provided in Section 4. Section 5 draws conclusions.

2. Proposed domino circuit

Implementation of a wide fan-in OR gate designed using the proposed domino circuit are shown in Fig. 3. For the proposed domino circuit, unlike the conventional domino circuits, the pull-down network is disconnected from the output inverter to decrease voltage swing across the pull-down network and hence reduce the power consumption. In fact, as shown in Fig. 3, only one pull-down transistor M_2 is connected to the output inverter, while n-transistor is connected to the inverter in the n-bit OR gate designed using the conventional domino. Therefore, in the proposed domino circuit, input of the inverter or node *Dyn* still has full voltage swing and lower capacitance, while top and bottom nodes of the pull-down network (nodes *A* and *B*) has lower voltage swing and larger capacitance compared to the conventional domino circuits. As a result, power consumption of the proposed domino is reduced especially in the case of wide fan-in gates due to existing large capacitance on nodes *A* and *B*.

As shown in Fig. 3, the main idea of the proposed circuit is the use of the voltages across the pull-down network i.e., the voltage difference between nodes *A* and *B*. With respect to the input voltages, voltages of nodes *A* and *B* (V_A and V_B, respectively) will be determined. In case all the inputs are low and consequently no conductive path exists in the pull-down network, V_A will be greater than V_B. Otherwise, V_A will become approximately equal to V_B. Therefore, the output voltage is changed regarding to voltages of these nodes as follows

$$\text{If } V_A > V_B + V_{tp} \Rightarrow M_1: \ ON \text{ and } V_{Out} = 0 \tag{1}$$

$$\text{If } V_A \cong V_B \text{ and } V_B > V_{tn} \Rightarrow M_2: \ ON \text{ and } V_{Out} = V_{DD} \tag{2}$$

In the proposed domino circuit, transistors M_{p1} and M_{p2} precharge nodes *A* and *Dyn*, respectively and transistor M_{dis} discharges node *B*. In addition, transistor M_1 keeps the state of node *Dyn* in a different way to the conventional domino. In fact, conductance of the transistor M_1 is controlled by the use of the voltage across the pull-down network. Thus contention between M_1 as the keeper transistor and transistor M_2 is less than that of the conventional domino. Therefore, the delay and power consumption of the proposed circuit is decreased due to the

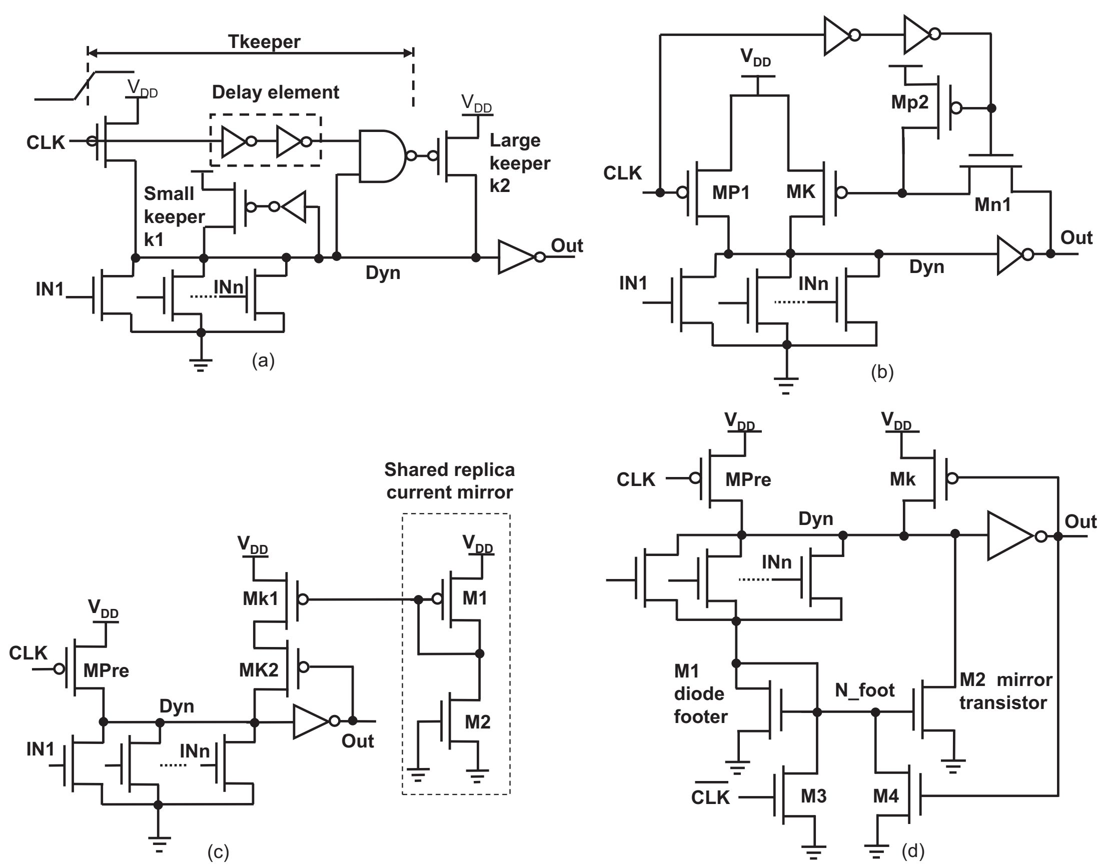

Fig. 2. Domino circuit techniques: (a) HSD [4], (b) CKD [5], (c) LCR [6], (d) DFD [7], (e) CCD [8], (f) VCD [9].