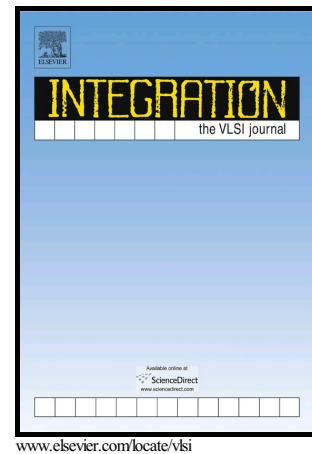# Author's Accepted Manuscript

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Design and Application of a CMOS Active Inductor at Ku Band based on a multi-objective optimizer

Mrinalinee Pandey[1,2], António Canelas[1,2], Ricardo Póvoa[1,2], Jorge Alves Torres[1,3], J. Costa Freire[1,2], Nuno Lourenço[1,2], Nuno Horta[1,2]

[1]Instituto de Telecomunicações, Lisbon, Portugal
[2]Instituto Superior Técnico – ULisbon, Lisbon, Portugal
[3]Academia Militar, Lisbon, Portugal
mrinalinee.pandey@ist.utl.pt
nuno.horta@lx.it.pt
antonio.canelas@lx.it.pt
rpovoa@lx.it.pt
jtorres@lx.it.pt
jcf@lx.it.pt
nlourenco@lx.it.pt

Abstract

This paper presents a new design of a grounded active inductor (AI) with an improved topology based on Manetakis regulated cascode active inductor comprising of three control voltages for tunability. An additional pMOST was introduced in the design as a drain load at the output of nMOST source follower. The aim of this work is to design a CMOS AI at Ku band using AIDA-C, a state-of-the-art multi-objective multi-constraint circuit-level optimization tool. Firstly, a reasonable AI operating at Ku band was manually designed using a 130 nm technology. This circuit and its design variables were fed to AIDA-C as an element of the initial population. Then the sizing of the proposed AI MOSTs was optimized. AIDA-C circuit sizing tool is able to achieve not only one but a set of solutions for the AI exhibiting high quality factor at a predefined Ku band operating frequency. This set of alternative Pareto optimal solutions enables the designer to choose the most suitable circuit sizing for a given application. AI's main performance parameters in terms of s parameters (s_{11}), quality factor (Q), inductance value (L), linearity, noise figure, power consumption and tunability based on control and biasing voltages are presented. Layout of the optimized AI is also presented. This AI was used to design active filters. Their selectivity, insertion losses and noise analysis is presented and discussed.

Keywords: Active Inductors; Ku Band; CMOS; Active Filters; multiobjective; optimizer

I. INTRODUCTION

Today's increasing demand and growth of wireless communications has boosted the research in the field of radio-frequency integrated circuit (RFIC) design and CMOS technology due to its advantage of shrinking design sizes and full integration of RF, Analog and Digital electronics on the same chip. Inductors with high Q (quality factor) are the key components of filters and VCOs (Voltage Controlled Oscillators). The technology is drifting towards the on-chip components for size and cost reduction. Thus we are looking for high quality on-chip inductors, as off-chip inductors are bulky and costly. Q of passive monolithic inductors decreases with frequency. Grounded active inductors (AI) are better than their passive counter parts in terms of Q, inductance tunability and low chip area. In the last three decades, two major types of active inductors have been reported for RF, microwave and more recently millimetre-wave: in the first approach, the inductors are realized with only active circuits; in the second approach, the inductors are realized by passive circuits and the active circuits are used only for the compensation of the losses of passive inductors. Since the second approach uses the passive spiral inductors, they require larger silicon area as compared to the first approach. Therefore, we have used the first approach that leads to smaller circuits. Implementation of CMOS AIs operative at Ku band frequencies using this approach has not been reported till now.

We cannot overlook the fact that CMOS active inductors may not compete with their passive counterparts in terms of noise, non-linearity and obviously dynamic range. However, they allow frequency tuning and chip area reduction in many applications. They also need DC biasing and the power consumption of the CMOS circuits cannot be neglected.

The race into smaller nanometer-scales and an increase in the device density poses new challenges in the RFIC design process. A reduced time-to-market imposes the use of advanced Computer Aided Design (CAD) tools to support the design task.

The aim of this work is to design a CMOS AI at Ku band using AIDA-C design automation methodology.