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A lifetime-aware analog circuit sizing tool

Engin Afacan *, Gonenc Berkol, Gunhan Dundar, Ali E. Pusane, Faik Baskaya

Bogazici University, Department of Electrical and Electronics Engineering, Turkey

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ABSTRACT

Reliability of CMOS circuits has become a major concern due to substantially worsening process variations and aging phenomena in deep sub-micron devices. As a result, conventional analog circuit sizing tools have become incapable of promising a certain yield whether it is immediately after production or after a certain period of time. Thereby, analog circuit sizing tools have been replaced by better ones, where reliability is included in the conventional optimization problem. Variation-aware analog circuit synthesis has been studied for many years, and numerous methodologies have been proposed in the literature. On the other hand, to our best knowledge, there has not been any tool that takes lifetime into account during the optimization. Besides, there are a number of different issues with lifetime-aware circuit optimization. For example, aging analysis is still quite problematic due to modeling and simulation deficiencies. Furthermore, a challenging trade-off between efficiency and accuracy is revealed during lifetime estimation in the optimization loop. Relatively expensive aging analysis is carried out for each candidate solution corresponding to a large number of simulations, so it is extremely important to deal with this trade-off. With regard to aforementioned these problems, this study proposes a novel lifetime-aware analog circuit sizing tool, which utilizes a novel deterministic aging simulator with adjustable step size. Hot Carrier Injection (HCI) and Negative Bias Temperature Instability (NBTI) mechanisms are considered during the lifetime analysis, where the NBTI model was developed via accelerated aging experiments through silicon data. As case studies, two different OTA circuits are synthesized and results are provided to discuss the proposed tool.

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1. Introduction

Analog circuit design has become a very time consuming process to be performed manually, where increased non-idealities complicate circuit analysis and lead to challenging trade-offs among different performance metrics [1]. To palliate this challenge, several design automation tools for analog circuit sizing have been proposed in the last two decades [2–10]. However, increasing variability and aging problems with developing technology have brought the yield of manufactured ICs as a major design objective as well as other electrical specifications. Conventionally, the lifetime period of a circuit can be examined under three distinct regions: *Infant Mortality*, *Regular Lifetime*, and *Wear-out* [11]. *Infant Mortality* corresponds to circuits having considerably high failure rates, where particular fabrication tests are assigned to weed out such devices before they come to market. At the end of this period, a certain yield is guaranteed thanks to variability-aware circuit design methodologies. Furthermore, yield analysis has been successfully incorporated into the conventional optimization problem [12,13]; thus, solutions with desired yield and confidence levels can be automatically generated. During the *Regular Lifetime* period, the remaining circuits operate properly for a long time until Wear-out, where aging begins. In the Wear-out period, circuits begin to lose their functionality, finally ending up with circuit malfunction after a certain time, as illustrated in Fig. 1.

Aging is a time-dependent process and aging analysis (modeling, simulating, and observing the aging effects) is relatively difficult to perform compared to variation analysis. The most relevant effect of aging is increase in the threshold voltage; so a typical aging evaluation is based on simulating circuits while increasing the threshold voltage as a function of operation time. However, an accuracy problem manifests itself during aging simulations due to the model inaccuracy and time-dependency of aging phenomena. Semi-empirical models that are generated via accelerated aging tests (AAT) [14–16] may generate more accurate estimations for a given technology. On the other hand, operating points of the circuit also change over time, so the amount of electrical stress on transistors change. Thereby, performing long-term reliability simulations within a single and long step may cause prediction errors. To overcome this problem, some commercial tools such as MOSRA (Synopsys), UDRM (Mentor), and

* Corresponding author.
E-mail address: engin.afacan@boun.edu.tr (E. Afacan).

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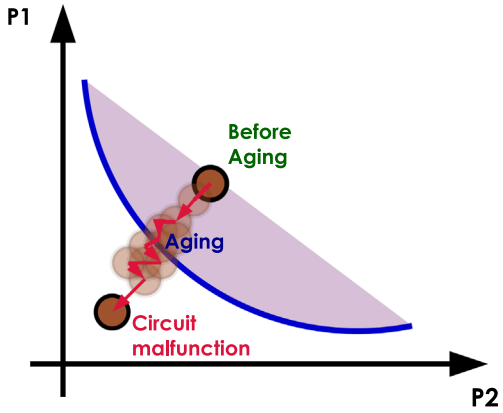

Fig. 1. Aging causes performance malfunction after a certain lifetime.

RelXpert (Cadence) divide the total simulation time into a number of intervals, calculate degradation amount, and update transistor parameters at the end of each interval. Nevertheless, these tools also have disadvantages. Firstly, such tools generally utilize low level aging models, which may lead to accuracy problems. In addition to that, using a static step size during long-term simulations can cause either inaccuracy or inefficiency, where larger time steps may cause prediction errors, and smaller steps increase the simulation time. Especially, considering numerous evaluations of candidate circuits during optimization, efficient reliability simulations become vital to reduce the total synthesis time. This paper proposes a novel lifetime-aware analog circuit optimization tool. Regarding aging simulation problems, a deterministic and dynamically sized aging simulator was developed. The proposed simulator utilizes a semi-empirical model for the NBTI phenomenon, where the model was developed through accelerated aging measurements on a test chip. Two different OTA topologies were chosen as synthesis examples, and synthesis results are given and discussed in detail.

The paper is organized as follows. In Section 2, a brief background on aging mechanisms in CMOS circuits, modeling of aging phenomena, and semi-empirical model development are provided. The developed aging simulator is introduced in Section 3. Section 4 presents the proposed lifetime-aware analog circuit synthesis tool. Synthesis results are provided and discussed in Section 5. Finally, Section 6 concludes this paper.

2. Background: aging phenomena in cmos

The continuous downscaling of CMOS technologies results in increased internal electric fields and current densities, which lead to higher stress on transistors and metal lines, and result in faster degradation. Hot Carrier Injection (HCI) and BTI (Bias Temperature Instability) are the most common reliability issues in CMOS technology. HCI occurs due to carriers accelerated by horizontal electrical field throughout the channel. These hot carriers cause impact ionization at the end of the channel, where an electron–hole pair is generated and electrons move towards the $Si-SiO_2$ interface, resulting in an increase in the threshold voltage. Conventionally, p-type devices do not suffer from HCI, because holes are majority carriers, and have lower mobility (and thus speed) compared to carriers (electrons) in n-type devices, which substantially decreases the probability of the impact ionization event.

On the other hand, BTI is caused by high vertical field across the channel, where charges at the channel are trapped by either pre-existing or post-generated interface states. As a result, these trapped charges lead to an increase in the threshold voltage. Charge trapping is known to be considerably less for p-type devices than n-type devices, so positive BTI (PBTI) effects can also be neglected for technologies above 45 nm. However, increasing usage of high κ devices, in which charge trapping has a higher potential compared to conventional SiO_2, PBTI may still take place [14,17]. In summary, although underlying mechanisms are quite different from each other, HCI and negative BTI (NBTI) manifest themselves as an increase in the threshold voltage of n-type and p-type devices, respectively. Therefore, conventional aging models are based on the estimation of the shift in the threshold voltage.

2.1. Modeling of aging effects

Analytical models and semi-empirical models have been utilized to estimate the aging effects. The most common analytical models have been proposed in [18], which are given in (1) and (2) for HCI and NBTI, respectively.

$$\Delta V_{th} = \frac{q}{C_{ox}} N_{it}$$
$$N_{it} = K\sqrt{C_{ox}(V_{gs}-V_{th})}\, e^{\left(\frac{E_{ox}}{E_0}\right)} e^{\left(-\frac{\varphi_{it}}{q\lambda E_m}\right)} t^n \tag{1}$$

$$\Delta V_{th} = \delta_v + \sqrt{K_v^2 (t-t_0)^{0.5} + \Delta V_{th0}^2} \Rightarrow Stress$$
$$\Delta V_{th} = (\Delta V_{th0} - \delta_v)[1 - \sqrt{\eta (t-t_0)/t}] \Rightarrow Recovery$$
$$K_v = A t_{ox} \sqrt{C_{ox} V_{ov}} (1 - V_{ds}/\alpha V_{ov}) \exp\left(\frac{E_{ox}}{E_0}\right) \exp\left(\frac{-E_c}{kT}\right) \tag{2}$$

Here, t is time, N_{it} is the number of interface traps, φ_{it} is the barrier energy, and K, E_0, λ, α, m, and n are technology independent parameters. The NBTI model covers both recovery and stress phases for long term operation, where $\alpha, \eta, E_c, A, E_0$, and δ_v are technology independent parameters, which are provided in [19]. A detailed discussion on these analytical models can be found in [18].

Apart from these analytical models, there are a number of semi-empirical models [20,21,16,22,23], where some specific accelerated aging tests are employed to obtain a projection of aging effects within shorter times. According to the semi-empirical models, HCI and BTI mechanisms are typically modeled with a power law dependence on the stress time t as

$$\Delta V_{th} = f(V_{GS}, T, W, L) \cdot t^n$$
$$\frac{\Delta I_d}{I_d} = f(V_{DS}, T, W, L) \cdot t^n. \tag{3}$$

The dominant source of the degradation is electrical stress on devices (V_{GS} and V_{DS}), but it also depends on absolute temperature (T), transistor dimensions (W, L), and time (t).

2.2. Accelerated aging test and semi-empirical model development

It is not practical to perform aging experiments under nominal conditions, where several months, or even years, are needed to develop a semi-empirical model. Instead, the state of the art procedure is performing measurements under elevated temperature and voltages, which is called Accelerated Aging Test [24]. It is a well-known fact that aging phenomena are accelerated with increased thermal and electrical stresses. Hence, the behavior of devices can be extrapolated and modeled. Conventionally, semi-empirical models are utilized for accelerated tests for both HCI and NBTI. Semi-empirical equations for the change in the threshold voltage of PMOS due to NBTI and the drive current for NMOS degradation due to HCI are given in (4) and (5), respectively.

$$\Delta V_{th} = B.(V_{gs})^{m_1}.e^{\frac{-E_a}{kT}}.L^{m_2}.W^{m_3}.t^{m_4} \tag{4}$$

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