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Automatic generation of test infrastructures for analog integrated circuits by controllability and observability co-optimization

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ABSTRACT

This paper presents a method to address the automatic testing of analog ICs for catastrophic defects. Based on Design-for-Testability building blocks offering extra controllability and extra observability, a test infrastructure is generated for a targeted circuit. The selection of the extra blocks and their insertion into the circuit is done automatically by a workflow based on DC simulations and optimization algorithms. Adopting a defect-oriented methodology, this approach maximizes the fault coverage while minimizing the silicon area overhead and test time. The proposed method is applied to two industrial circuits in order to generate optimal test infrastructures combining controllability and observability. These case studies show that, with a silicon area overhead of less than 10%, a fault coverage of 94.1% can be reached.

1. Introduction

The testing of analog Integrated Circuits (ICs) has been a center of focus for many years. While advances in this field have been made, the challenge of testing analog ICs in an automated way still remains. At the same time, electronics continues to extend its presence in various domains and leads engineers to face new quality requirements. For instance, the automotive industry combines nowadays an average of 400 ICs per vehicle and intends to increase this number in the future with, for instance, the expected arrival of self-driving cars. Since the defect probabilities of all components of a system multiply with each other, the requirement on each component increases and defect levels below the part-per-million (ppm) are desired. These tightening quality requirements combined with a shortening time-to-market put pressure on IC designers and manufacturers. Therefore, an advancement is needed in the testing of analog ICs and its automation.

The testing of digital ICs has known an automation of its process and an improvement leading to defect levels under the ppm. This success was made possible by using a fault-based approach and by the appearance of automated algorithms such as PODEM [1] or FAN [2]. Furthermore, a generic Design-for-Testability (DfT) approach based on flip-flops connected in a scan chain was developed and enabled the automatic utilization of these algorithms.

In comparison, the field of analog IC testing has not yet known this same level of automation. Currently, research has delivered Built-In Self-Test (BIST) structures which focus on the testing of specific types of circuits (ADC/DAC, PLL, etc.) [4,3], but no automated tool is at the designers' disposal to enable the testing of analog circuits like the digital scan chain does in digital ICs.

The problem of testing analog circuits in a generic way has been addressed in works such as [5,6] where analog scan chains are proposed. In the same way as in digital scan chains, voltages can be scanned through sample-and-hold (S/H) circuits and imposed on node voltages. Similarly, node voltages can be read and scanned out of the chips by chains of S/H circuits. While these methods tackle the testing of analog circuits in a generic approach, they suffer from several drawbacks. The parasitics imposed on the probed nodes by the analog buses have been criticized. Also, the forcing of voltages on internal nodes requires the presence of multiple buffers. The whole approach requires a significant silicon area overhead.

In this paper, a method is proposed to automatically generate a DfT infrastructure in order to test analog ICs. The presented method combines small building blocks offering extra controllability and extra observability to the circuit under test (CUT). This co-optimization of controllability and observability offers an alternative to the analog scan chains without requiring a large silicon area. This paper comes as an extension to a work previously presented [7]. A more detailed description of that implementation is given here and new considerations are implemented.

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In Section 2, the defect-oriented methodology enabling the method is summarized. Then, the building blocks forming the basis of the method are presented in Section 3. In Section 4, the workflow of the method is presented from the DC simulations to the combination of the building blocks through an optimization system. In Section 5, two industrial circuits are taken as case studies and simulations results are shown. Finally, conclusions are drawn in Section 6.

2. Defect-oriented method

In the defect-oriented approach, the physical defects which can occur in ICs are considered and are simulated with fault models [10,9,8]. Defects can be distinguished into two categories: catastrophic and parametric defects. The former emerge from a problem during the manufacturing process such as an over- or under-etching, the presence of a dust particle, etc. They cause a modification of the designed topology i.e. a short circuit or an open circuit. The latter emerge from an imperfect control of the process, voltage and temperature (PVT) conditions. These PVT variations cause variability among the produced ICs, resulting in some ICs laying outside of the targeted specifications. In the scope of this work, the focus is put on automotive applications where the used technologies are typically above 100 nm and hence are mastered well enough to apply a 6σ design flow. Therefore, parametric defects are under control and only catastrophic defects are considered in this work.

The modeling of the defects is done at schematic level with models from literature [11]: the 5-fault model for the MOSFETs and the 6-fault model for the bipolar transistors. The application of these models on a circuit C_0 results in a list of faults $F_1,\ldots,F_n$. Then, one by one, the faults from the generated list are separately inserted into the original circuit C_0. The insertion of a fault F_i into the circuit C_0 leads to the faulty circuit C_i. The transistor-level simulation of the circuit C_i allows to estimate the effects of the fault on the circuit. The method developed in the following makes use of results coming from these DC simulations in the presence of process variations.

3. Controllability and observability structures

In this section, the concepts of controllability and observability are introduced as defined in [12]. The controllability is defined as the relative difficulty of setting a node to a specific value. The observability is defined as the relative difficulty of measuring the signal value at a node. The combination of these two concepts forms the basis for an optimized way to test an analog integrated circuit. The main idea is to control a circuit and lead it into a region of operation where a different behavior can be observed between a faulty circuit and a good circuit.

In the following, two techniques are presented in order to enhance the controllability and the observability of analog ICs. The controllability is enhanced by using the Topology Modification method introduced in [9]. The observability is enhanced by using the Local Detection and Transmission Systems introduced in [11]. The combination of both techniques provides a simplification of the test infrastructure as compared to analog scan chains. As a result, DfT Control and Observation Structures (COS) can be generated to test analog ICs with a small silicon area overhead.

It is worth noting that no specific hypothesis is made about the considered circuit. However, both DfT techniques require extra-circuitry to be connected internally into the CUT. Therefore, the presented method is more suitable for low-frequency circuits such as the ones encountered in the automotive or biomedical industries. Circuits such as RF circuits can suffer from performance degradation due to the extra-parasitics introduced by the DfT blocks. In that case, the use of non-intrusive DfT techniques is advised and has been proposed in literature [13].

In the scope this work, the consideration of the sensitive nodes has been simplified by allowing the designers to make a pre-selection of the circuit nodes. The sensitive nodes of the circuit are therefore removed from the nodes to be considered and are not used by the two DfT methods. In the future, the analysis of the effects of the added parasitics will be automated and included in the workflow.

3.1. Topology modification

The Topology Modification method consists in reconfiguring the targeted CUT to make defects observable. In [14], the modification of the value of some circuits components is used as a form of reconfiguration. In the scope of this work, the topology of the CUT is modified by means of small transistors added to the original circuit. These transistors are either connected between a node of the circuit and the ground (pull-down transistor), or a node of the circuit and the voltage supply (pull-up transistor), as illustrated in Fig. 1. In the following, when the distinction between a pull-down (PD) and pull-up (PU) transistor is of no importance, the general denomination PX is adopted. The insertion of the PX transistors in the original circuit C_0 leads to the set of topologies $\{T_0, T_1, \ldots, T_p\}$, where T_0 is the original circuit C_0.

During the generation of these alternative topologies, two aspects have to be taken into consideration: the sizing of the used PX transistors and the stress imposed to the circuit when these are activated. After trials on the case studies from Section 5, it has appeared that minimal sizing for the PX transistors delivers convincing results. For what concerns the induced stress, the modified topologies are simulated and it is verified that they operate in the safe operating area (SOA) defined for the technology. The topologies which lead to excessive currents flowing through circuit branches are removed from the list of usable topologies.

During the normal operation of the circuit, the PXs are deactivated and hence do not have any effect on the circuit, besides the small capacitive parasitics inherent to their presence. During the test mode, these PX transistors are individually activated in order to make the CUT adopt different topologies. In the scope of this work, these modified topologies emerge from the activation of only one PX element at a time. The simultaneous activation of multiple PXs could be considered and would lead to more compact and more efficient solutions. However, this benefit would come at

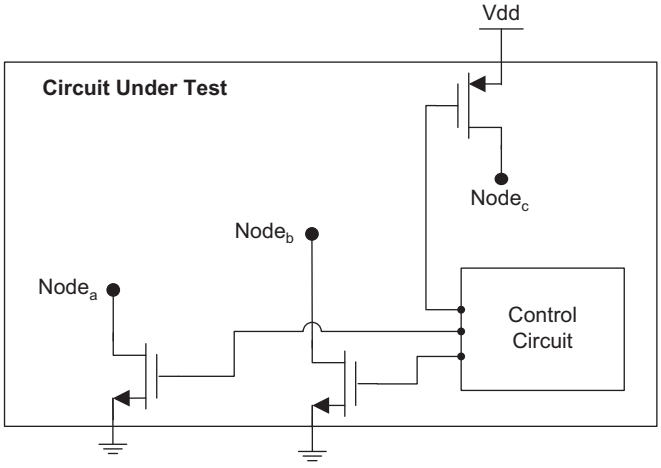

Fig. 1. Block diagram representation of the proposed test infrastructure.

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