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On the convex formulation of area for slicing floorplans

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ABSTRACT

In this paper, it is shown that the area optimization problem of a compact slicing floorplan may be formulated as a convex optimization problem when the areas of the analog components are modeled with continuous convex functions of the width (height). It is proved that the area of a compact slicing floorplan is a convex function of its width (height). The convexity is shown for the cases with and without dead (empty) space. This feature can be exploited to efficiently optimize the dimensions of layout components with multiple variants, without enumerating all possible combinations. Layout of a voltage-doubler circuit is used to quantitatively verify the proof.

1. Introduction

Reducing iterations between different design levels has been suggested by the International Technology Roadmap for Semiconductors as a major contribution towards the reduction of design cost. Towards this end, the integration of physical and electrical synthesis in one single step has been proposed, yielding the so-called layout-aware circuit synthesis approaches, such as [1]. Most successful analog circuit synthesis approaches are based on the formulation of the sizing problem as an optimization problem, commonly solved by iterative processes that imply hundreds or thousands of circuit performance evaluations. It becomes obvious that integration of physical synthesis into such circuit synthesis process is only practical if the circuit layout can be instanced very fast.

A key step of the physical synthesis process, and essential to determine layout area, is the layout floorplanning, i.e., the determination of properties and spatial relationships of a set of blocks. Lots of approaches have been reported along the three past decades for floorplanning of many (usually digital) cells in a chip [1–10].

Automatic floorplanning of analog circuits is less complex than its digital counterpart in terms of the number of blocks involved. However the complexity comes from analog constraints such as symmetry or proximity. Most reported approaches have focused on area minimization meeting some analog constraints [11,12]. However, an essential aspect in area minimization of a given analog floorplan is the variant selection problem, i.e., the determination of the specific implementation of each block among a set of possible realizations.

This paper deals with slicing floorplans. A floorplan is called slicing [2], if it is possible to recursively split it into rectangular slices by means of successive horizontal and vertical cuts. The resulting slices may be represented by a binary tree.

Area optimization on slicing analog floorplans using shape functions [3] (i.e., piece-wise linear functions built by instancing a device generator for discrete parameter values) accounting for every variant realization of component blocks was done in [1]. Enhanced shape functions were used in [4] for non-slicing floorplans. In both, shape functions were constructed by enumerating all possible solutions, therefore, a costly process if the number of variants is high. This optimization problem could be more efficiently solved if it could be formulated as a convex optimization problem. A function $f(x)$ is called convex, if it satisfies the condition:

$$f(\theta \cdot x+(1-\theta)\cdot y) \le \theta \cdot f(x)+(1-\theta)\cdot f(y) \quad (1)$$

where $\forall x, y \in \mathbf{dom} f$ and for all $\forall \theta \in \mathbf{R} : 0 \le \theta \le 1$. For continuous functions, a non-negative second derivative also indicates convexity:

$$\frac{d^2}{dx^2}[f(x)] \ge 0 \quad (2)$$

where $x \in \mathbf{dom} f$ and $f(x)$ is a twice differentiable function.

A relevant property of convex functions is that they have a single minimum, thus, if a minimum is found, it is the global minimum. Therefore, very efficient optimization algorithms can be applied and there is no risk to get stuck at local minima.

There is a one-to-many mapping from an analog device to its layout, i.e., a device may be represented by different layouts, commonly known as variants, by changing its geometrical

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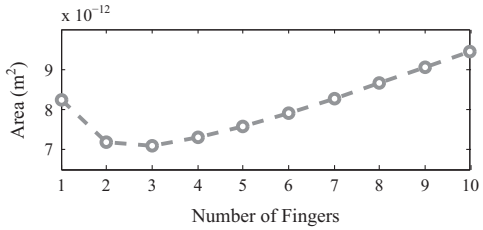

Fig. 1. The area of a transistor changes as the number of fingers *m*changes. Each data point corresponds to a different *m* value for a transistor in the UMC 0.13 μm technology with $W=5$ μm and $L=0.5$ μm.

parameters. For example, by changing the number of fingers of a transistor, different layouts may be obtained. For illustration's sake, Fig. 1 shows the area of a single transistor for different number of fingers, hence, different variants. In previous approaches to analogous problems, the transformation $\theta \leftrightarrow e^{\theta}$ was used and it was shown that after this transformation the problem of area optimization for a fixed floorplan is convex [5–7] and the transformed problem may be efficiently solved with a geometric programming solver. In these works, the area of each block was assumed to be constant for all possible variants. However, this is not the case for analog layouts as illustrated in Fig. 1. Also, these works did not consider the analog constraints. Note that symmetric placement constrains cannot be formulated in a geometric program.

A related work [8] demonstrates that the minimum area floorplanning problem is not convex and its optimal solution cannot be obtained by solving its Lagrangian dual problem. However, this is only the case if the heights of the blocks are not constrained by their widths.

We define a layout as *compact* if for a given width (height), it is not possible to obtain a shorter (thinner) layout by changing the geometrical parameters. For instance, the layout of Fig. 2a is not compact for the defined width *w*, if there exists a shorter layout, as in Fig. 2b. If the layout of Fig. 2b is the shortest possible layout, we call it a compact layout for the given width *w*. The concept of compactness is visualized in Fig. 2c, where the area of a layout and the area of a compact layout are represented by the filled region and the dark solid line, respectively.

In this paper, the width and height of a combination are denoted by *w* and *h*, respectively. The symbol ψ is used to denote the area of a combination. The area of a *h*orizontal combination, as in Fig. 3, is denoted by ψ_{H} whereas the area of a *v*ertical combination, as in Fig. 4, is denoted by ψ_{V}. Depending on the context a second index is used to denote *e*qual ($\psi_{\mathrm{H_E}}$ or $\psi_{\mathrm{V_E}}$), ma*x*imum ($\psi_{\mathrm{H_X}}$ or $\psi_{\mathrm{V_X}}$) and mi*n*imum ($\psi_{\mathrm{H_N}}$ or $\psi_{\mathrm{V_N}}$).

In this work we prove that the total area of a compact slicing floorplan is a convex function of its width (alternatively height). It is also shown that the convexity is satisfied, without applying any transformation and without any assumption on constant area. The proof makes only two assumptions on the component blocks:

- The area of a block is a convex function of its width (height), which is the case for analog devices such as resistors, capacitors and, transistors [9].
- Height $h(w)$ (alt. width $w(h)$) is a non-increasing function of the width w (alt. height h). In other words, the wider the variant is, the shorter the height is. This is also the case for analog devices [9]. Formally stating:

$$\frac{d}{dw}[h(w)] \le 0 \tag{3}$$

From this point, the width *w* is accepted as the free parameter and the height $h(w)$ is used as a continuous function of the width.

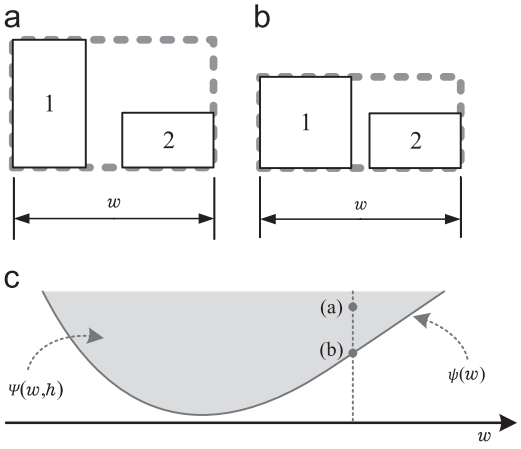

Fig. 2. Layout (a) is not compact, if it is possible to obtain a shorter layout as in (b) for a given width *w*. Points representing the areas of (a) and (b) are shown in (c). Filled region in (c) represents the area of any layout $\Psi(w,h)$ and the dark solid line represents the area of a compact layout $\psi(w)$.

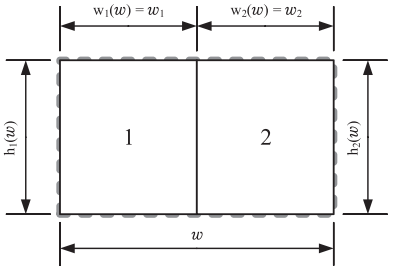

Fig. 3. Horizontal combination without dead space: heights of the blocks are equal, this configuration is denoted by $\mathrm{H_E}$ (*h*orizontal-*e*qual-height).

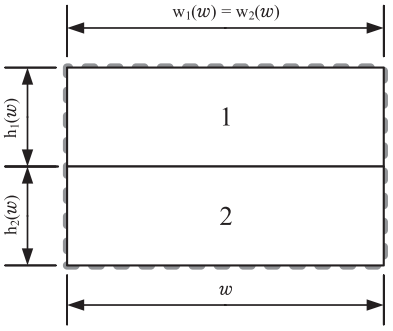

Fig. 4. Vertical combination without dead space: widths of the blocks are equal, this configuration is denoted by $\mathrm{V_E}$ (*v*ertical-*e*qual-width).

By observing a few instances of a device generator and also using the models in [9], height of a device may be easily formulated as a continuous function of its width. All the results may be obtained, without loss of generalization, if the height *h* is considered as the free parameter and the width $w(h)$ is used as a function of the height. Throughout the paper, if not explicitly stated, the dimensions of the blocks are assumed to be independent.

Our proof demonstrates that the area of a compact layout with two blocks is convex and can be extended to any compact slicing floorplan. Layouts without and with dead space are considered in Sections 2 and 3, respectively. In Section 4, our proof is generalized to any compact slicing floorplan. The proof is experimentally verified in Section 5. The conclusion is given in Section 6.