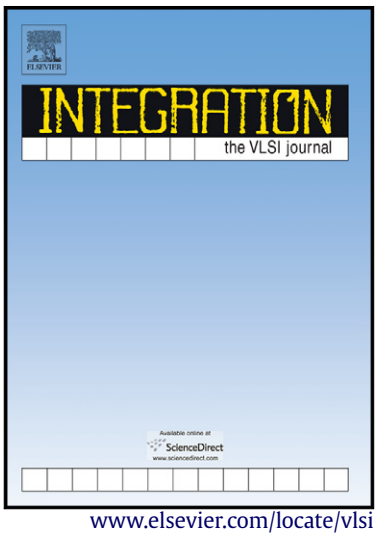

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On the Design of Hybrid Routing Mechanism for Mesh-based Network-on-Chip

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Abstract

Efficient on-chip communication is necessary for exploiting enormous computing power available on a many-core chip. Routing algorithms play a major role for the communication quality and performance of the on-chip interconnection networks. This paper proposes TagNoC, as an on-chip network router architecture with novel hybrid routing approach which reduces latency and power consumption at a fixed cost based on information redundancy. TagNoC is a hybrid routing approach which combines the source and distributed routing methods together. While eliminating packet routing in each router, TagNoC determines the forwarding output port in parallel with input buffering. For a marginal cost increase in header size, as compared to distributed routing techniques, routing latency can be hidden while eliminating power consuming portion of the routing, increasing router throughput and decreasing latency. The proposed TagNoC router is compared to baseline router with distributed routing implementation on a 16-node CMP mesh. Physical implementation of all routers is modeled using synthesized RTL, detailed area analysis, and accurate channel models. Performance evaluation is also carried out utilizing RTL simulation and detailed power analysis on both synthetic and application traffic is performed using post-synthesis gate-level simulation. The simulation results illustrate that TagNoC outperforms as compared to baseline distributed architecture and other source routing methods in terms of power, latency, and throughput.

Keywords: Network-on-Chip, Source Routing, Tag, Power, Distributed Routing

1. INTRODUCTION

The traditional high clock rate single core systems have been replaced by distributed many-core systems on a single die due to energy consumption and performance limits. Data transmission through a chip is considered more difficult since global interconnects are becoming the principal performance bottleneck for high performance systems [22, 24]. System-on-Chip (SoC) does not support future technologies as the number of cores on single dies increases. Network-on-Chip (NoC) has been proposed as a new interconnection architecture to support better modularity, scalability and higher bandwidth features [2, 7, 17, 19]. Power dissipation is becoming critical constraints of system design due to battery lifetime, cooling, and thermal budgets concerns [5]. It has been reported that network power for a many-core die in the future can be as high as 150W, assuming current network scale implementations [3]. Reducing energy consumed in NoC is of great importance for high performance and energy-efficient designs [4, 28, 35].

Routing is an integral part of NoC, and has a significant impact on the communication efficiency, especially in case of single-flit packets [12].

Routing algorithm can be implemented as source or distributed routing. In source routing method the complete path from source to destination is precomputed at source router and accumulating the exact router-to-router packet traversal information in the header. This information leads the packets to traverse through intermediate routers toward their destination, which has reasonable overhead for small networks. The header of the packet needs to contain at most k units of routing information for a network with a diameter of k. The header overhead becomes noticeable as the network size grows which is a big challenge for on-chip routing. However, the routing decision is made by the individual routers in distributed routing method, in which the header of a packet requires to contain only the destination address. The destination address is compared in each intermediate router to choose the appropriate channel to forward the packet. The router complexity of the latter scheme is higher than the former one though it imposes scalable information redundancy [9].

Although distributed routing is the most common technique in NoC, this paper TagNoC, as an hybrid routing method, showing superior performance along with saving area or power, by adding fixed number of bits (only one bit per dimension) which is called *Tag*.

Major contributions of this article are:

- Propose a new hybrid routing technique to reduce the intrinsic overhead of conventional source routing and per-hop running of distributed routing methods.
- Provide a detailed implementation of the proposed technique,TagNoC, with comprehensive scalability, performance, power, frequency, and area analysis.

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