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Research paper

Metal work function engineering on epitaxial (100)Ge and (110)Ge metal-oxide-semiconductor devices

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ABSTRACT

Capacitance-voltage characterization of epitaxial *n*-type (100)Ge and (110)Ge metal-oxide-semiconductor capacitors (MOS−Cs) was performed using two work function Al and Pt gate metals to evaluate the orientation effect on flat-band voltage (V_{FB}) shift, Fermi level pinning factor (S), and interface induced defects (D_{it}). These epitaxial (100)Ge/AlAs/GaAs and (110)Ge/AlAs/GaAs heterostructures were grown *in-situ* using two separate molecular beam epitaxy (MBE) chambers. A V_{FB} shift of > 700 mV, S > 0.5, and D_{it} value of ~ $6 \times 10^{11}\,cm^{-2}\,eV^{-1}$ in the energy range of 0.05 eV to 0.3 eV below the conduction band, have been demonstrated from epitaxial *n*-type (100)Ge and (110)Ge surfaces, which are comparable to the reported bulk Ge MOS-C values, suggesting a robust MOS-C developed process as well as device quality epitaxial (100)Ge and (110)Ge layers on GaAs substrates using an AlAs intermediate buffer. Thus, the metal work function engineering on device-quality MBE grown crystallographically oriented Ge materials, can offer a promising path for extending the performance and application of Ge-based field-effect transistors for low-power devices.

1. Introduction

The replacement of polysilicon gates with metal gates in silicon (Si) metal-oxide-semiconductor field-effect transistors (MOSFETs) at the 45 nm transistor node has engendered a lot of interest in the metal work function engineering of MOSFETs [1] for continued transistor miniaturization. For *n*-channel and *p*-channel MOSFETs, two distinct gate metals are generally used to accommodate for the difference between the metal work function, φ_m, and the semiconductor work function, φ_s (which differs for *n*- and *p*-type channels), φ_{ms}. φ_{ms} has a direct impact on the flat-band voltage (V_{FB}), which in turn affects the transistor threshold voltage (V_{TH}). However, the ability to tune V_{FB} using two different work function metals in a metal-oxide-semiconductor capacitor (MOS−C) configuration, and consequently V_{TH}, is limited by Fermi-level pinning (FLP) at the semiconductor's surface. This FLP stems from the formation of a dipole layer, shown in Fig. 1, originating from intrinsic surface states that have been filled due to the presence of charged interfacial defects [2] at the oxide/semiconductor heterointerface. The formation of an additional dipole layer at the metal/oxide heterointerface is also possible, corresponding to the well-described metal-induced gap states, *i.e.*, the filled intrinsic oxide surface states resulting from the evanescent coupling of the metal electron wave function and available oxide surface states. [3, 4] The influence of these dipole layers depends on the cumulative difference between φ_m and the charge neutrality level φ_{CNL} at the semiconductor surface, as shown in Fig. 1, where $E_{F,m}$ is the Fermi-level energy of the metal and E_{CNL} is the charge neutrality level (CNL) energy level, *i.e.*, the *effective* Fermi-level energy at the semiconductor surface. The interface dipole(s) that forms alters the interfacial band alignment, generating significant band bending at the semiconductor surface in order to equilibrate E_{CNL} and $E_{F,m}$, thereby altering φ_m and producing $\varphi_{m,eff}$, the effective metal work function. $\varphi_{m,eff}$ can be expressed by the following: [5]

$$\varphi_{m,eff} = \varphi_{CNL} + S(\varphi_m - \varphi_{CNL}) \quad (1)$$

where S is known as the Schottky pinning parameter, which ranges from 0 (full pinning) to 1 (no pinning). If MOS-C's implementing different gate metals [5–7] are fabricated from the same oxide/semiconductor structure, the difference in flat-band voltage, ΔV_{FB}, is now equivalent to the difference in $\varphi_{m,eff}$, *i.e.*, $\Delta\varphi_{m,eff}$. Correspondingly, Eq. (1) can be re-written in terms of ΔV_{FB}, S, and the difference in effective metal work functions:

$$\Delta V_{FB} = \Delta\varphi_{m,eff} = S\Delta\varphi_m \quad (2)$$

In this work, the integration of two different gate metals, platinum (Pt) and aluminum (Al), to form MOS-Cs on (100) and (110) crystallographically oriented epitaxial Ge heterostructures grown by solid

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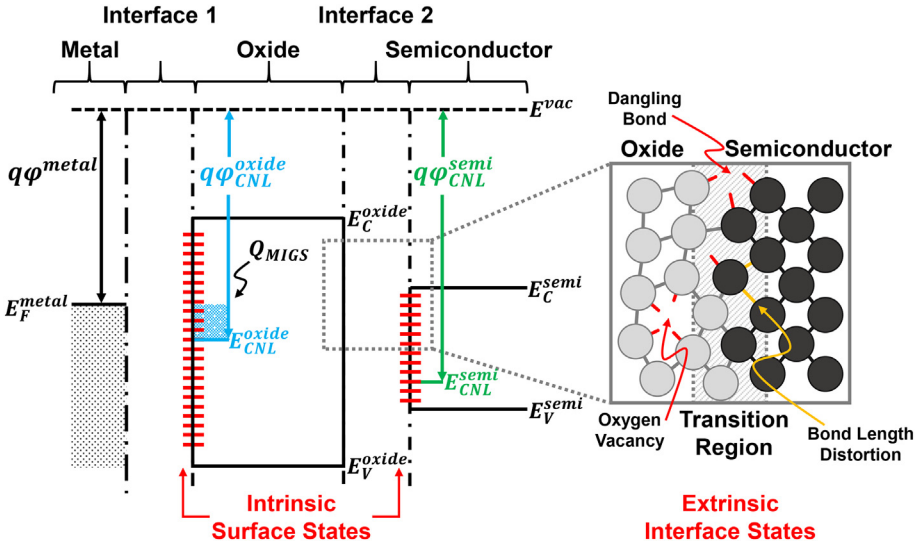

Fig. 1. Schematic energy band diagram of a metal-oxide heterointerface and the intrinsic interface states that form due to differing charge neutrality levels (CNLs) between the dissimilar materials (adapted from Ref. [5]). It also illustrates the intrinsic and extrinsic surface states at each heterointerface.

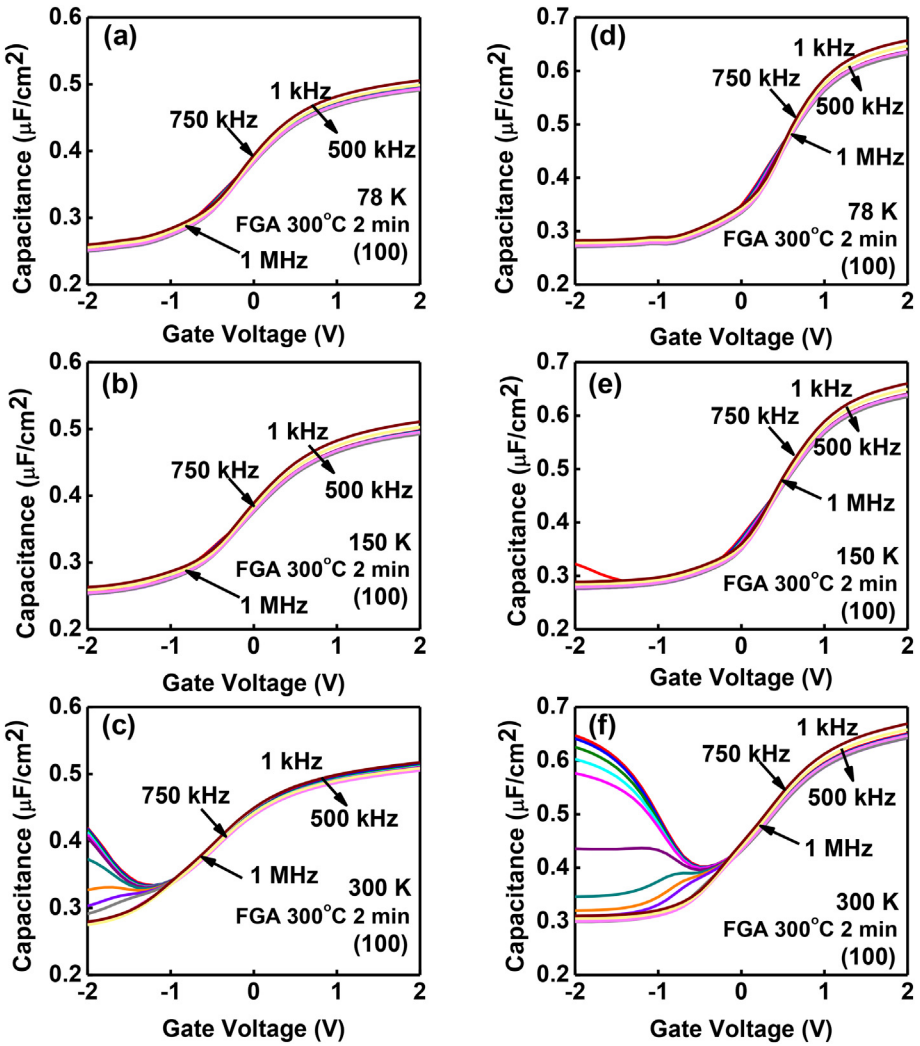

Fig. 2. C–V characteristics of the (100) Ge MOS-C on GaAs *via* an AlAs buffer architecture using two different gate metals. Devices with 100 nm Al/0.4 nm TiN measured at (a) 78 K (Ref. [10]), (b) 150 K and (c) 300 K. Devices with 60 nm Au/40 nm Pt/0.4 nm TiN measured at (d) 78 K, (e) 150 K and (f) 300 K.