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Research paper

# Understanding the influence of in-plane gate electrode design on electrolyte gated transistor

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ABSTRACT

Present work investigates the influence of gate electrode design in performance of electrolyte-gated carbon nanotube transistors. Electrolyte gated transistors have a huge potential in biological and chemical sensing. Recently, in-plane gate electrode has replaced the earlier used gate electrode wire in these systems. It becomes extremely essential to investigate the impact of gate electrode design on the device properties, and to optimize the electrode design to harness maximum sensitivity and speed. As a part of this work we have investigated the impact of gate electrode area and the distance between the gate electrode and the channel on the transistor characteristics. Area of gate electrode scales almost linearly with the drain to source current. However, the dependence of the gate distance is highly affected by experimental factors. Random network of carbon nanotubes serve as the semicondutor channel for electrolyte gated field effect transistors under study.

## 1. Introduction

Electrolyte gated field effect transistors (EGFETs) have several distinctive features, the most important being the low operating voltages (< 1 V), suited for small scale integration with in-vitro systems and the possibility of operating in physiological solutions make them highly suitable for biosensing applications [1]. In such devices the semiconductor at the channel is exposed directly to the aqueous media without the need of an encapsulation layer [2]. The capability to work in sub-1 V supply is due to the higher electric double layer capacitances developed at the liquid-semiconductor and liquid-gate electrode interfaces, which are in the order of μF/cm$^2$ compared to nF/cm$^2$ of standard dielectrics [3].

A major research on EGFETs is focused, on the material studies of novel semiconductors and electrode metals [4, 5] or on the nature of electrolyte [6]. There are very few studies that focus on the impact of electrode design on the device performance. Recently an in-plane gate design is used in EGFETs, where the gate electrode is fabricated in the same lithography step as the source and drain electrodes. As a part of this study we explore the effect of varying dimension of the in-plane gate electrode on the device characteristics of the EGFETs, with the intention of optimizing the device design and achieve maximum speed and sensitivity.

Random network of carbon nanotubes are used as semiconductor channel. Due to their extraordinary electrical, mechanical, and chemical properties, single-walled carbon nanotubes (CNTs) have been extensively explored for a number of electronic applications [7, 8, 9,10, 11]. Solution processable random network CNTFETs have demonstrated high mobilities and the high current densities that can be obtained at low voltages, hence making them suitable candidates for applications including flexible displays, interactive sensor networks and biochemical sensors [12,13,14].

## 2. Experimental

The area of the active channel in the two device layouts, used in this study, is fixed to 2.5 mm$^2$. To study the impact of varying gate area, the equidistant gate electrodes are placed around the channel with gate area to channel area ratios as 0.17:1, 1:1, 2:1, 4:1 and 6:1. To study the impact of distance between gate and channel, the equal area gate electrodes are placed at distances 4.5 mm, 5.5 mm, 6.5 mm, 7.5 mm and 8.5 mm away from the channel. Fig. 1(A) and (B) show schematic representation of these two layouts.

The electrolyte gated CNTFETs are fabricated on flexible kapton substrate. Source, drain and gate electrodes are patterned in one photolithography step followed by thermal evaporation of 50 nm gold(Au) contact metal and 5 nm of chromium(Cr) as adhesion promoter layer between gold and the substrate. The interdigitated source drain

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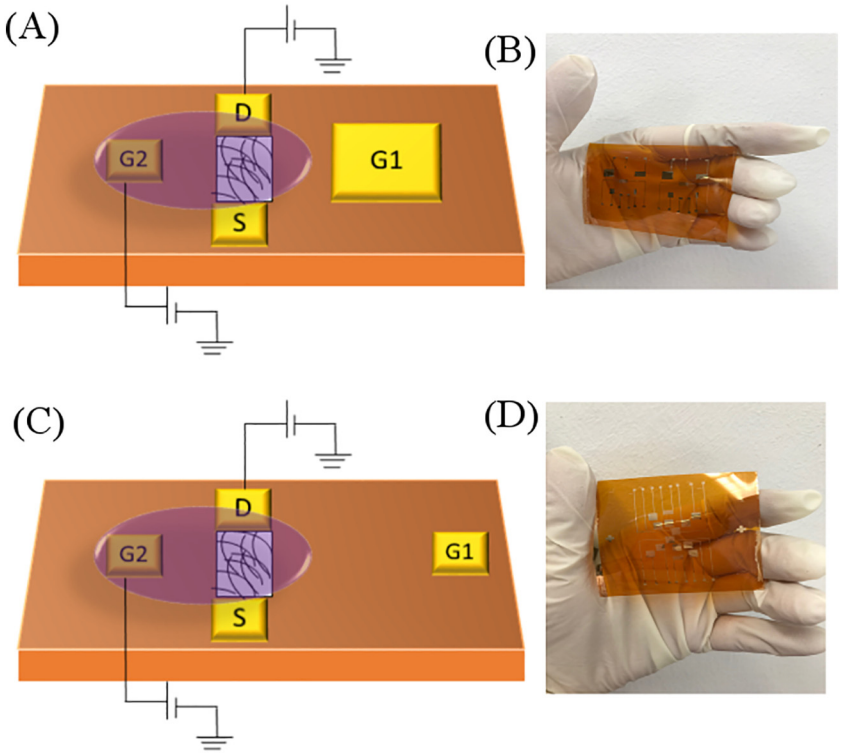


**Fig. 1.** Schematic representing: (A) two gate electrodes(G1 and G2) with different areas and equidistant with the semiconductor channel, and (C) two equal area gate electrodes(G1 and G2) at varying distance from the semiconductor channel. Devices used to studying impact of (B) gate area and (D) distance between gate and channel, on device characteristics.

electrode structure (IDES) have a channel length of 60 μm and channel width of 3000 μm. Post liftoff, a second lithography step is performed to passivate the contact metal lines which will allow precise control on the ratio of the area of semiconductor channel and the gate. In the final step, 90% semiconducting CNT solution is sprayed over the IDES using a shadow mask. The CNT solution is prepared [15] by dispersing CNTs in an aqueous medium surfactant sodium dodecyl sulfate (SDS). As a final step to remove the surfactant from the single-walled CNT(SWCNT) network the samples are immersed in DI-$H_2O$ for 15 min.

## 3. Results and discussion

The CNTFETs are electrically characterized using Keithley SCS 4200. During the electrical measurements 100 μl of phosphate buffer solution (PBS) purchased from Sigma Aldrich is dropped on the FETs such that the electrolyte covers the channel and gate electrode completely.

Fig. 2(A) shows the transfer curves for five devices prepared on the same channel but varying gate areas. For these measurements the gate to source voltage ($V_{GS}$) is swept from 0.8 to −0.8 V and drain to source voltage ($V_{DS}$) is fixed to −0.1 V. The use of voltages below ± 1 V is to avoid any water hydrolysis or other electrochemical reaction at the gate electrode or the semiconductor surface [16]. With increasing applied $V_{GS}$ in the negative direction there is increase in drain current $I_D$, indicating a p-type response for the CNTFET. As seen in Fig. 2(A) the maximum on-current of the transistor increases with increasing gate area. The increase in the electrode area leads to increase in double layer capacitance and hence a stronger gate control, as expressed in eq. 1.

$$I_D = \mu^* C^* \frac{W^*}{L}\left[(V_{GS} - V_t)V_{DS} - \frac{{V_{DS}}^2}{2}\right] \quad (1)$$

Transconductance ($g_m$) defined as $dI_D/dV_{GS}$, is an important characteristics widely used to indicate improved gate control [17] in field effect transistors. Fig. 2(B) is a plot of transconductance with varying $V_{GS}$ for different gate electrode areas. The maximum transconductance ($g_{m,\ max}$) for the FETs is obtained at biases closer to the maximum $V_{GS}$ and the value of $g_{m,\ max}$ increases with the gate area.

To investigate further the impact of the gate electrode area on other transistor characteristics, multiple devices are measured and four major transistor characteristics namely maximum drain current, on-off ratio, hysteresis and maximum transconductance are studied. Fig. 3 shows the percentage change in these properties with varying gate area. Fig. 3(A) shows the change in the on-current with the increase in gate areas. The on current increases almost linearly with the increase in the gate electrode area. This is because $I_D \propto C$ (double layer capacitance), which in turn is linearly related to the gate electrode area. This dependence is also seen in the relative change of the on/off ratio (Fig. 3(B)) and transconductance (Fig. 3(C)) with the gate electrode area, as these two

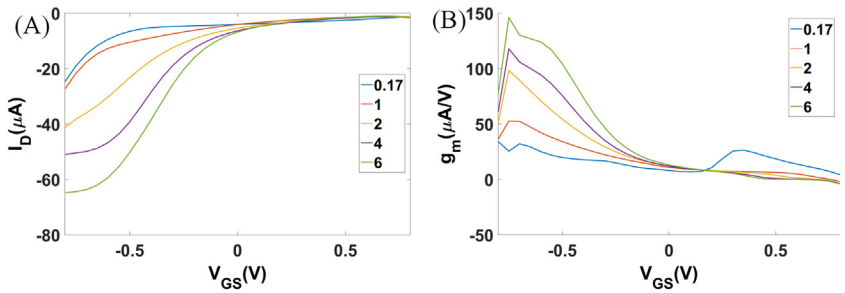


**Fig. 2.** (A) Transfer characteristics and (B) transconductance vs $V_{GS}$, for five transistors fabricated on the same channel with different gate electrode area.