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Calibration of offset via bulk for Low-power HfO_2 based 1T1R memristive crossbar Read-Out System

C. Mohan[a], L.A. Camuñas-Mesa[a], E. Vianello[b], L. Periniolla[b], C. Reita[b], J.M. de la Rosa[a], T. Serrano-Gotarredona[a] and B. Linares-Barranco[a]

Seville, Spain

Instituto de Microelectrónica de Sevilla, IMSE-CNM (CSIC/Universidad de Sevilla)[a,], CEA-LETI[b]*

[a]*Parque Científico y Tecnológico, Cartuja, Calle Américo Vespucio, s/n, 41092 Seville*
[b]*17 Avenue des Martys, 38054, Grenoble*

Abstract

Neuromorphic RRAM circuits typically need currents of several mA when many binary memristive devices are activated at the same time. This is due to the low resistance state of these devices, which increases the power consumption and limits the scalability. To overcome this limitation, it is vital to investigate how to minimize the amplitude of the read-out inference pulses sent through the crossbar lines. However, the amplitude of such inference voltage pulses will become limited by the offset voltage of read-out circuits. This paper presents a three-stage calibration circuit to compensate for offset voltage in the wordlines of a memristor-array read-out system. The proposed calibration scheme is based on adjusting the bulk voltage of one of the input differential pair MOSFETs by means of a switchable cascade of resistor ladders. This renders the possibility to obtain calibration voltage steps less than 0.1mV by cascading a few number of stages, whose results are only limited by mismatch, temperature, electrical noise and other fabrication defects. The system is built using HfO_2-based binary memristive synaptic devices on top of a 130-nm CMOS technology. Layout-extracted simulations considering technology corners, PVT variations and electrical noise are shown to validate the presented calibration scheme.

Keywords: Memristor, neuromorphic, crossbar, nano-CMOS, calibration

*Corresponding author

Email address: mohan@imse-cnm.csic.es (Instituto de Microelectrónica de Sevilla, IMSE-CNM (CSIC/Universidad de Sevilla))