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# Area-efficient ferroelectric multi-bit memory device

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## Abstract

Owing to both ferroelectricity and polymer properties, ferroelectric polymers are suitable for fabrication of high-density memory devices in a multi-layered structure. Recently, multi-bit memory devices using a ferroelectric polymer has been reported, in which two capacitors in a memory cell are horizontally positioned and they are electrically connected in a parallel. In this paper, however, a multi-bit memory device with multi-layered structure will be demonstrated, in which two capacitors are vertically positioned but they are electrically connected in parallel, equivalently. By blending crosslinking agent into ferroelectric solution, organic-solvent-tolerant ferroelectric film could be realized for vertically-stacked structure. The memory operation was observed at a maximum of 20 V, and there were four distinct states. In particular, the area efficiency of 25% is higher than that of a previous horizontal multi-bit memory device. The findings here are expected to be very useful to those involved in the creation of high-density and high-reliability organic memory devices.

**Keywords:** ferroelectric polymer, multi-bit memory, area efficient memory, multilayer

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