

Accepted Manuscript

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Hasan Hosseinzadeh, Saeed Rasouli Heikalabad



PII: S0167-9317(18)30036-4
DOI: <https://doi.org/10.1016/j.mee.2018.01.019>
Reference: MEE 10710
To appear in: *Microelectronic Engineering*
Received date: 7 September 2017
Revised date: 25 November 2017
Accepted date: 24 January 2018

Please cite this article as: Hasan Hosseinzadeh, Saeed Rasouli Heikalabad , A novel fault tolerant majority gate in quantum-dot cellular automata to create a revolution in design of fault tolerant nanostructures, with physical verification. The address for the corresponding author was captured as affiliation for all authors. Please check if appropriate. Mee(2017), <https://doi.org/10.1016/j.mee.2018.01.019>

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A novel fault tolerant majority gate in quantum-dot cellular automata to create a revolution in design of fault tolerant nanostructures, with physical verification

Hasan Hosseinzadeh, Saeed Rasouli Heikalabad*

Department of Computer Engineering, Tabriz Branch, Islamic Azad University, Tabriz, Iran

*Corresponding author, s.rasouli@iaut.ac.ir

Abstract

There are some challenges in CMOS circuits, one of the most important of which is the size of the feature. Alternative technologies such as quantum-dot cellular automata (QCA) are emerging to solve this problem. In QCA, the scale of main structures is very small, which can cause faults. There are several ways to overcome this problem. One of them is the design and use of the fault-tolerant majority gates. The majority gate is one of the most widely used components in designing QCA structures. In this paper, we propose a new fault-tolerant majority gate. We investigate the performance of the proposed structure when common faults occur, and then we compare the results with previous structures. Using this structure, we propose a new structure for a fault-tolerant full-adder. QCADesigner is used to implement and simulate proposed structures. Physical verification is used to confirm the results.

Keywords:

Quantum-dot cellular automata (QCA); Fault-tolerant; Majority gate; Full-adder; Nanotechnology

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