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Research paper

A drain leakage phenomenon in poly silicon channel 3D NAND flash caused by conductive paths along grain boundaries

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ABSTRACT

In this paper, a new drain leakage current phenomenon in the polycrystalline silicon channel three-dimensional (3D) NAND flash cell is discovered, which we have modeled as "leakage paths along the grain boundaries". This drain leakage current increases sharply with the growth of channel diameter, and a current increasing phenomenon under voltage stress appears in the device with large drain leakage current. This leakage current can adversely affect memory operation, and reduces device-to-device uniformity. Based on our model, we can alleviate the effect of this phenomenon by optimizing polysilicon formation process and channel polysilicon thickness.

1. Introduction

3D NAND flash technology develops rapidly to overcome scaling bottleneck of conventional planar NAND flash [1–4]. In 3D NAND flash, polycrystalline silicon is the typical channel material instead of monocrystalline silicon in planar NAND flash. Compared with planar NAND flash device, the reliability of polycrystalline silicon channel is a major concern [5–7]. This reliability issue is caused by grain boundaries and randomly distributed defects in polysilicon channel, and becomes one of the most important issues of 3D NAND flash. Previous work shows that carriers are trapped in grain boundaries, and form potential barrier between crystalline grains, impeding current from crossing the grain boundary [8,9]. Although the trapped carriers hinder current across the grain boundary, they can collect dopant and form conductive paths along grain boundaries. No previous work has studied the impact of this effect.

In this work, we study the conductive characteristic of polycrystalline silicon systematically, and discover some abnormal phenomena including leakage current increasing trend with channel diameter and current increasing under voltage stress. We propose a conductive model to explain these properties of polycrystalline silicon channel: conductive paths exist along the grain boundaries, and raise channel leakage current. And we also offer suggestions to structure and process design based on our model.

2. Devices fabrication and electrical properties

We fabricated a polycrystalline silicon channel gate-all-around (GAA) vertical transistor to study the properties of polycrystalline silicon. Fig. 1 shows the structure of our test device and the main manufacturing process steps. Devices are fabricated by gate-first and channel-last approach by patterning cylindrical holes with a depth of 300 nm (including 50 nm bottom oxide, 200 nm poly silicon control gate and 50 nm top oxide). About 10 nm thick SiO_2 gate dielectric is deposited at the sidewall. Gate stack is capped with a thin amorphous silicon layer before spacer etching, to protect the oxides during the opening of the bottom of the hole, and the polysilicon channel is formed by LPCVD after bottom etching. The upper end and substrate is n+ doped to lower the resistance. We design five sets of devices with different channel diameters, from 60 nm to 100 nm, to study the influence of channel size.

A standard transistor characteristic can be observed in our devices: the on/off ratio is over 10^6(Fig. 1b). In this paper, to compare electrical characteristics of devices with different diameters, we define the drain current under −2 V gate voltage and 1 V drain voltage as drain leakage current and drain current under 8 V gate voltage and 1 V drain voltage as drain saturation current.

We measure the conductive properties of 65 devices for each channel diameter, and analyze the effect of channel diameter. Fig. 2 shows the statistical distribution of the drain leakage current and drain saturation current. It can be observed that when hole size increases from 60 nm to 100 nm, the median of leakage current increases for more than 10^6 times, while the saturation current increases less than 10 times (Fig. 2c and d). The drain saturation current increases linearly on the channel sectional area, but the leakage current increases sharply with channel diameter. We consider that conductive paths along grain boundaries lead to this phenomenon.

To study the reliability issue of polysilicon channel further, we measure the drain current dependency with stress time, and discover a gradual current increasing phenomenon under drain voltage stress in device with large channel diameter, and this phenomenon is not

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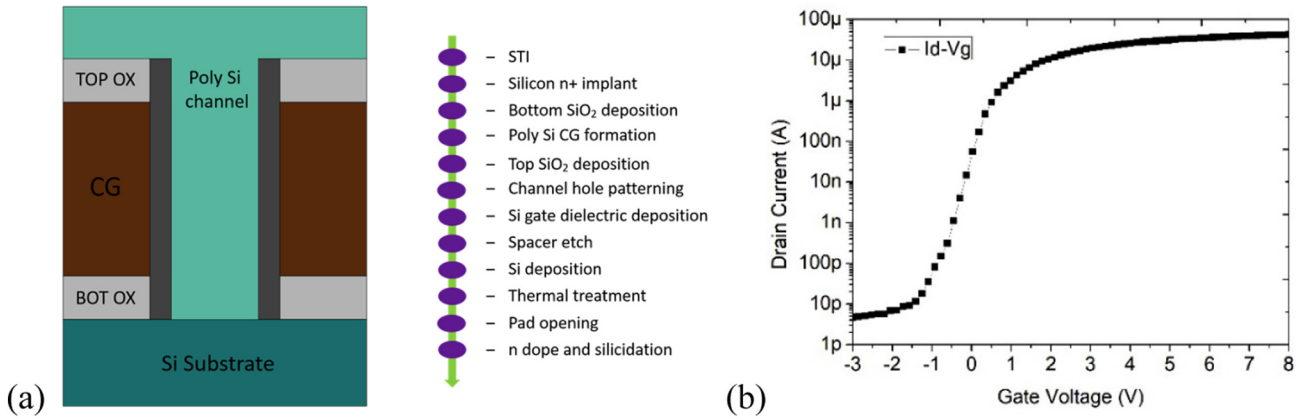

Fig. 1. (a) Schematic view of our vertical single test vehicle and simplified manufacturing process steps (b) $I_d - V_g$ ($V_d = 1$ V) characteristics of our test device.

shown in device with small channel diameter (Fig. 3). After applying drain voltage, drain current increases slowly for about 50 s, and then remains stable. This phenomenon is reversible. If the drain voltage stress is removed for over 100 s, the device recovers to the initial state, and will repeat the current increasing phenomenon again under stress.

3. Proposed model

To explain these phenomena, we propose a conductive model: grain boundaries in polysilicon form leakage paths, and these leakage paths are responsible for the sharp increase of drain current and gradual current increasing phenomenon under stress [10].

Grain boundary is the main cause to unreliability of polycrystalline silicon conduction. Previous works mainly focus on the impeding effect of grain boundaries to the current across grain boundaries. We infer that conductive paths along grain boundaries (Fig. 4a) exist besides regular conductive paths across grain boundaries (Fig. 4b) in poly silicon channel. Because of the impurity concentration in grain boundary and irregular structure, the leakage path along grain boundaries can lead to a lower resistance, which is identical to our measurement. And a

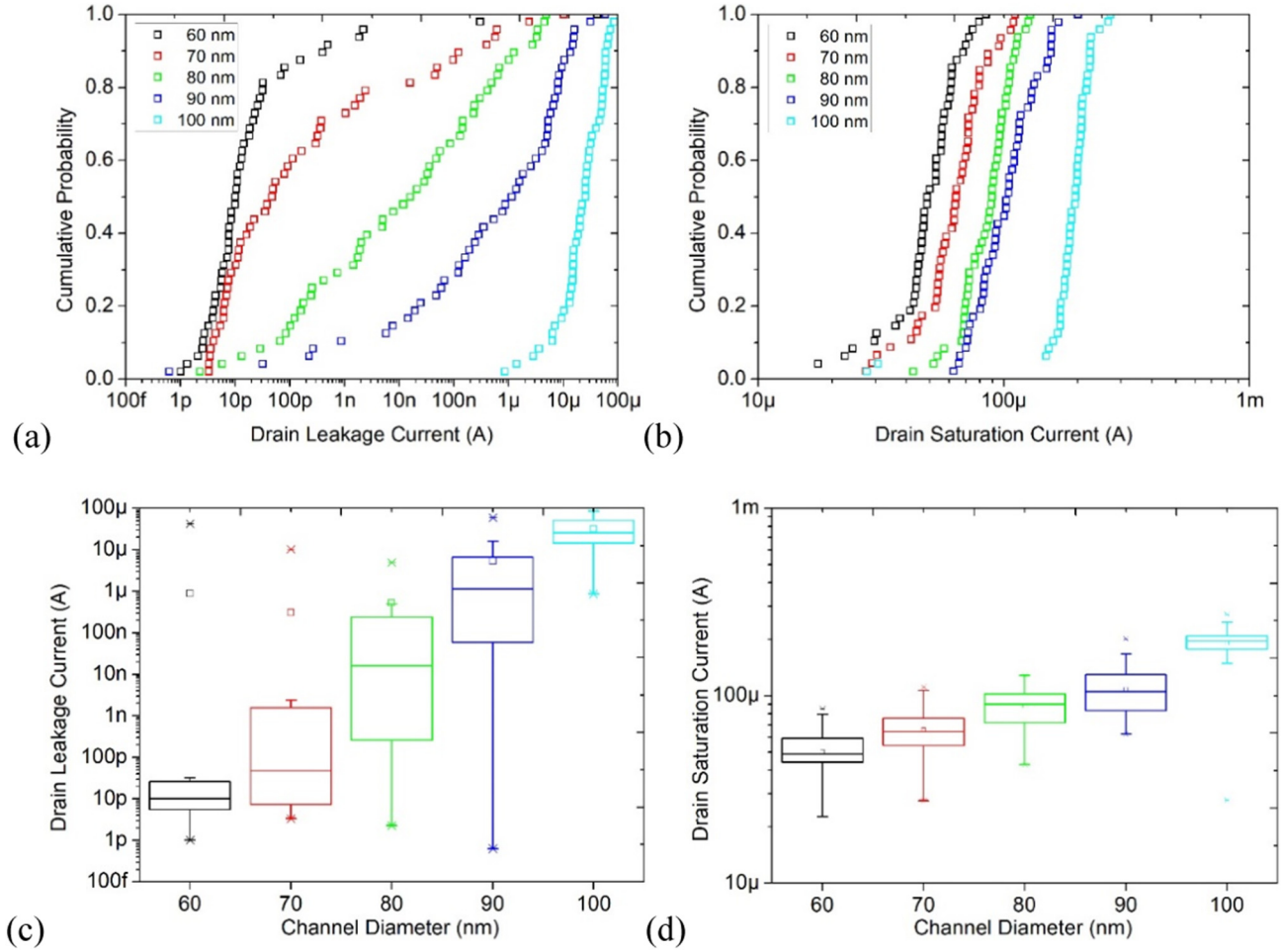

Fig. 2. (a) Cumulative distribution function of drain leakage current. (b) Cumulative distribution function of drain saturation current. (c) Drain leakage current distribution of devices with different channel diameters. (d) Drain saturation current distribution of devices with different channel diameters.