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A Novel Wet Etching Based Double-Sides Interposer Structure with Deep Trenches for 3-D Hetero-Integration

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Abstract

Through-silicon-via (TSV) interposer has been proved to be a good solution for three-dimensional integration to achieve high density and improved performance. In this paper, a novel double-sides silicon interposer structure with deep trenches was proposed to achieve high density 3-D hetero-integration. The TSVs in the interposer were fabricated by wet etching method on both sides, which has low cost, good reliability and suitable for batch production. In order to minimize the TSV size and provide a higher interconnect density as well as retain the mechanical reliabilities of the interposer, deep trenches were wet-etched before TSV fabrication, which were also used for chip embedding. To further increase the integration density, multiple interconnects were attempted to be deposited in a single TSV and their electrical properties were systematically characterized.

Keywords: 3D integration; Silicon interposer; Anisotropic wet etching; Trench.

1. Introduction

Three-dimensional (3D) integration technologies are being widely developed to address the ever continuing device miniaturization, system-level integration and performance promoting for the needs of mobile and digital applications [1-3]. 3D integration requires a physical stacking of die onto another die or substrate with vertical through-silicon-vias (TSVs) serving as the interconnects. TSV interposer has been envisioned to be a good solution for 3D hetero-integration to achieve high density interconnections, improved electrical performance and increased data bandwidth due to shorter interconnects between the dies, and to minimize coefficient of thermal expansion (CTE) mismatch induced stress between the dies and the interposer [4, 5].

To fabricate the TSVs, dry anisotropic etching methods such as deep reactive ion etching (DRIE)