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Co and $CoTi_x$ for contact plug and barrier layer in integrated circuits

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ABSTRACT

Continuous transistor scaling in integrated circuits brings about a significant increase of electrical resistance in the source/drain area. To alleviate the problem, this paper proposes Co/$CoTi_x$ to replace conventional contact plug/barrier materials of W/TiN/Ti. Co and $CoTi_x$ amorphous alloy layers were deposited on SiO_2/p-Si. The 3 nm-thick amorphous $CoTi_x$ layer promoted adhesion between Co and SiO_2. The resistivity of the 150 nm-thick Co film on $CoTi_x$ showed low film resistivity close to bulk Co value both in as-deposited and annealed conditions. The amorphous structure of the $CoTi_x$ layer was maintained throughout annealing up to 500 °C. Capacitance-voltage measurement of Co/$CoTi_x$/SiO_2/p-Si samples showed a good diffusion barrier property of the $CoTi_x$ layer between Co and SiO_2 after thermal stress as well as bias thermal stress. The obtained results indicated that Co/$CoTi_x$ can be good candidate materials for contact plug and diffusion barrier in advanced integrated circuits.

1. Introduction

The device geometries for very large scale integrated circuits (VLSI) are under continuous pressure to miniaturize. As transistor channel length decreases, source/drain contact plug and M0 local interconnect are decreased in their size. Tungsten (W) has been used as a material for middle-of-the-line (MOL) which consists of contact plug and local interconnect due to its low thermal expansion coefficient and resistivity. The W in MOL is covered with Ti/TiN bilayer materials. The Ti layer is formed by physical vapor deposition (PVD), and is used mainly for creating low contact resistivity between W and Si [1]. In addition, The TiN layer is formed by chemical vapor deposition (CVD), and is used as an adhesion layer for CVD W and a barrier layer against chemical attack by the WF_6 precursor gas and other reactant gas species [2]. Inadequate protection leads to the formation of W volcanos, wormholes, delamination, and TiF_x-type compounds at the TiN/$TiSi_2$ interface [3]. With the advancement of technology node, the volume of W metal decreases and the resistance of W contact plug with high aspect ratios (AR) increases [4]. The obvious solution to achieve resistance reduction is to reduce the thickness of the underlying liner/barrier stack (Ti/TiN). Unfortunately, the Ti/TiN stack cannot be scaled any thinner because it cannot protect Ti from WF_6 attack and volcano defects and opens are created accordingly [5,6]. Another issue of the W MOL is related to the requirement of the nucleation layer by using a reducing agent of silane (SiH_4) [7] or diborane (B_2H_6) [8]. Poor step coverage of the nucleation layer leads to poor structural quality of the W contact plug. A thin nucleation layer would be preferred to minimize its influence on the W contact plug. However, too thin nucleation layer would lead to WF_6 attack. Various works have been conducted to alleviate these issues related to the nucleation layer by carrying out W deposition by plasma-enhanced CVD (PECVD) or ALD [9–12].

Possible solutions to the above mentioned scaling issues of the MOL are to switch W with other low resistance metals and to switch Ti/TiN with other liner/barrier materials. To find an alternative metal to W, we can consider bulk resistivity (ρ_0) and electron mean free path (λ). A metal with the lowest value of $\rho_0 \times \lambda$ product is expected to exhibit the highest conductivity in the limit of a small wire width. Promising metals in this regard are Mo, Co, and Ru, which have comparable $\rho_0 \times \lambda$ product to that of W with competitive processing and/or electromigration advantages [13]. Proper choice of precursor materials would not cause any chemical attack, thus, the Ti/TiN layer can be replaced with other materials.

Here, we propose Co as a lower resistance metal to replace W. Unlike W, Co metal does not need high resistivity nucleation layers and can be annealed at low temperature to undergo grain growth and reflow into high aspect ratio contact plug. There have been some previous reports on Co metallization. Kamineni et al. reported that switching from W/TiN/3 nm Ti to Co/TiN/2 nm Ti resulted in 2.5× line resistance reduction and this Co metallization showed void-free and seamless fill at the local interconnect level [14]. Wislicenus et al. measured the resistivity of a thin Co film deposited on CVD TaN_x barrier. They applied the Mayadas–Shatzkes model for thick films of 20 to 50 nm and the Namba model for thinner films to fit the measured data. Although, the resistivity of around 30 μΩ.cm was reported for 5 nm thick Co film,

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further reduction in resistivity could be obtained with higher quality Co films [15]. At 7 nm technology node with via and trench sizes below 15 nm, Co via and Cu line structure could eliminate Ta/TaN at via bottom, leading to the decrease of via resistance by 30% [16,17]. These properties of Co would bring about a lower contact and via resistance than conventional W for future technology node.

In this paper, we propose Co for contact plug and M0 local interconnect together with amorphous $CoTi_x$ alloy for liner/barrier. Recently, we reported that 3 nm thick amorphous $CoTi_x$ showed good adhesion, low resistivity and good barrier properties against Cu diffusion into SiO_2 [18]. Here, we extend our study of the amorphous $CoTi_x$ alloy as a barrier/liner layer for possible application to Co contact plug. Although, in actual device production, chemical vapor deposition would be carried out to form the $Co/CoTi_x$ structure, we employed a sputter deposition method. In this way, fundamental properties can be easily and systematically investigated by changing film thickness, composition and annealing condition. To the authors' knowledge, the performance of barrier/contact plug materials based on Co has not been established yet. In this work, the adhesion and barrier properties of $CoTi_x$ alloys as Co diffusion barrier under thermal and bias thermal stresses will be reported.

2. Experimental procedure

Co film (150 nm) and $CoTi_x$ thin film (3 nm) were deposited on SiO_2/p-type Si wafers by co-sputtering of two pure metal targets with a working pressure of 6×10^{-1} Pa and a 99.99% purity level of Ar gas flow at 15 sccm. The amorphous composition range of $CoTi_x$ was reported in our previous paper [18]. Adhesion strength of 150 nm-thick Co on SiO_2 and 400 nm-thick Co with 3 nm-$CoTi_x$ barrier was evaluated by tape test in accordance with ASTM D 3359–79 [19]. To evaluate the diffusion barrier property of the 3 nm-$CoTi_x$ film, the samples were annealed at various temperatures in Ar + 5%H_2 flow using a tube furnace. Film resistivity was measured by a four-point probe method. Structure, morphology and composition profile were investigated by cross-sectional high resolution transmission electron microscopy (HRTEM) and X-ray energy dispersive (EDX) spectroscopy. Cross-sectional HRTEM samples were prepared using a focused ion beam apparatus (FIB).

Capacitance-voltage (C-V) measurement was carried out on metal-oxide-semiconductor (MOS) samples before and after TS and BTS using a parametric analyzer (Keysight B1500A) operated at a frequency of 1 MHz at room temperature. The MOS samples were composed of a stacked structure of Co (150 nm)/$CoTi_x$ (3 nm)/th-SiO_2 (20 nm)/p-Si. The effectiveness of $CoTi_x$ as a diffusion barrier was studied by comparing the C-V curves of other MOS samples without the $CoTi_x$ layer. An ohmic contact electrode on the backside was made by locally removing oxide with diluted HF followed by deposition of a 500 nm-thick Al film by PVD. The top gate electrode of Co with or without $CoTi_x$ were formed using a lift-off technique [18]. Thermal stress (TS) tests were performed in an Ar + 5%H_2 flow tube furnace at temperatures of 250–700 °C for 10 min. For bias thermal stress (BTS) tests, a bias field of 3 MV/cm was applied at 250 °C for various times in an Ar + 5%H_2 flow microprobe system. After each set of the BTS tests during cooling to room temperature, the bias field was kept being applied to the samples to prevent back-diffusion of Co ions. The measured MOS capacitance (C_{MOS}) was normalized to oxide accumulation capacitance (C_{OX}) to compare flatband voltage (V_{fb}) shift with TS and BTS. The V_{fb} was calculated by plotting $1/(C_{MOS}/C_{OX})^2$ versus gate voltage [20]. Aluminum is considered a stable MOS metallization on thermally grown SiO_2 [21]. Hence it was used as a reference metal for Co diffusion studies.

3. Results

Table 1 lists the tape test results of as-deposited and annealed Co (150 nm) and Co (400 nm) films with or without $CoTi_x$ (3 nm) on SiO_2/Si. It is noted that the test condition is severe for the annealed thick film due to growth stress and thermal stress. Upon the test, the film was cut into 10 × 10 square regions. It is found that, without the $CoTi_x$ layer, only a few square regions are left after peeling off of the tape, indicating poor adhesion. On the contrary, with the 3 nm thick $CoTi_x$ layer, all 100 square regions remain intact, indicating good adhesion. The obtained results are expected because of strong chemical interaction of Ti with oxygen in the substrate [22].

Table 1
Tape test results.

Condition	Pass or fail		
	Co(150 nm)/SiO_2/Si	Co(150 nm)/$CoTi_x$(3 nm)/SiO_2/Si	Co(400 nm)/$CoTi_x$(3 nm)/SiO_2/Si
As dep.	Fail	Pass	Pass
250 °C, 10 min	N/A	Pass	Pass
400 °C, 10 min	N/A	Pass	Pass

Fig. 1 shows the film resistivity of Co with and without $CoTi_x$ after annealing at 250–800 °C for 10 min. By annealing up to 400 °C, the film resistivity decreases in both cases, owing to Co grain growth and defect annihilation. As annealing temperature increases to 800 °C for 10 min, the resistivity remains low around 7 μΩ.cm close to the Co bulk resistivity of 6.2 μΩ.cm. However, the resistivity of the Co film without $CoTi_x$ gradually increases, suggesting interdiffusion between Co and SiO_2.

High resolution TEM images reveal the change of the $CoTi_x$ layer by annealing at temperature range of 250–700 °C for 10 min. Prior to annealing, Fig. 2(a) indicates that the approximately 3 nm thick $CoTi_x$ layer has an amorphous structure. After annealing at 400 °C (Fig. 2(b)), the $CoTi_x$ layer stays amorphous and keeps its continuity. Composition profiles of the as-deposited and the 400 °C annealed samples both show that Co and Ti are located in the interface layer. After annealing at 500 °C (Fig. 2(c)), the thickness of $CoTi_x$ decreases to approx. 2.5 nm but it still has an amorphous structure in some areas. Further annealing at 600 °C resulted in more thickness reduction as well as the formation of some crystalline regions (Fig. 2(d)). In the composition profile, the Ti distribution shifts towards SiO_2 side which is accompanied with the separation of O from SiO_2. At 700 °C (Fig. 2(e)), the amorphous interface layer cannot be identified. The Ti distribution overlaps more with Si and O rather than with Co. For the Co profile, it is initially broad before annealing because of the overlapped distribution of Co in the $CoTi_x$ layer with the top Co film. With increasing annealing temperature, the Co intensity shows a steep increase from the interface towards the top Co film, indicating the separation of Co from the $CoTi_x$ layer and merging with the top Co film.

Fig. 3 shows C-V curves of MOS capacitors with and without 3 nm-thick $CoTi_x$ after thermal stress (TS) at various temperatures for

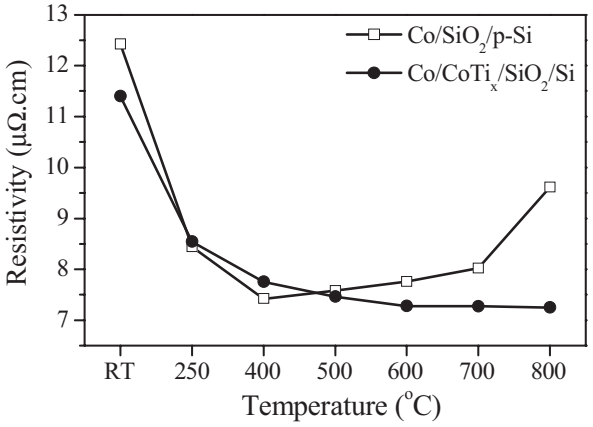

Fig. 1. Film resistivity of the Co/SiO_2/Si structures with and without $CoTi_x$ after annealing at various temperature for 10 min.