Microelectronic Engineering 189 (2018) 18–27

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Research paper

Fabrication of package embedded spiral inductors with two magnetic layers for flexible SIP point of load converters in Internet of Everything devices

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ARTICLE INFO

Article history:
Received 17 October 2017
Accepted 19 December 2017
Available online 20 December 2017

Keywords:
Point of load DC-DC converters
Internet of Everything
Embedded planar inductors
Flexible system in package
Stencil printing
Composite magnetic material

ABSTRACT

Inductive DC-DC converters are key elements in power delivery units for the development of Internet of Everything (IoE) architectures made of interconnected networks of smart devices, self-powered from different energy sources. The ultra-low power levels involved in IoE devices in addition to cost reduction of final products requires the development of new technologies for the miniaturization of all the active and passive components. In this paper, a low temperature, cheap and simple two-steps fabrication process of embedded planar inductors with two magnetic layers on a very thin, flexible and lightweight FR4 organic substrate is demonstrated for flexible System in package (SIP) based point of load DC-DC converters in IoE devices. The process uses standard printed wiring board (PWB) copper etching to define the square geometry of the planar inductors and trenches underneath the inductor copper traces. Very thick top and bottom magnetic layers are deposited using stencil printing of an FR4 compatible epoxy-NiZn ferrite composite magnetic material on top of the copper traces and into the trenches. At 30 MHz, the permittivity is 3.4 and 6.23 while the dielectric loss tangent is 0.014 and 0.009 for the epoxy and composite magnetic material respectively. The composite material has a permeability of 8.46, a loss tangent value of 0.1 at a frequency of 30 MHz and saturates around 0.13 Tesla. The DC resistance varies from 136 mΩ to 386 mΩ while at 30 MHz the AC resistance varies from 1.9 Ω to 10.1 Ω for an inductance value from 180 nH to 715 nH, corresponding to an inductance density between 5.69 nH/mm^2 and 12.47 nH/mm^2 and a quality factor between 13 and 17. Flexibility and its effect on the electrical parameters of the fabricated inductors is demonstrated through bending tests. A variation of <3% for the DC resistance is obtained for 5 mm bend radius. At 30 MHz and for a bend radius (both upward and downward) from 3.7 mm to 5 mm, the flat state (unbent) AC resistance and inductance values (1.9 Ω to 10.1 Ω for 180 nH to 715 nH) decrease by 6.5% to 18% and by 2% to 4.4% respectively which increase the self-resonant frequency by 3% to 3.4% and the quality factor by 2.2% to 20%. The characterized inductors are modeled in ANSYS HFSS electromagnetic simulator and simulation results show a good correspondence with the measured inductances and quality factors, which allows a reliable prediction of the inductors behavior for DC-DC converter design and implementation for IoE devices.

1. Introduction

The Internet of Everything concept aims at interconnecting a network of ultra-low-power smart objects (automotive vehicles, Home Automation, metering and Security systems etc.) and smart sensors for real time monitoring and/or decision-making. For an autonomous operation, these devices have to be self-powered and different powering schemes need to be implemented simultaneously such as batteries, energy harvesting from surrounding environment and wireless power transfer. The presence of different power sources at the same time in addition to different power consumption levels for a given operation mode (standby or active mode) imply voltage levels varying over a wide range. To ensure an optimal use of power for such situations, a power delivery/management system using switching mode DC-DC converters is required. Among the voltage converters topologies, inductive DC-DC converters, in which the inductor is the key power transfer element from input to the load represent the dominant architecture for high efficiency power delivery units [1–2]. Because of the small size and cost requirements for IoE applications due to the number of interconnected devices and very low power levels involved, special care needs to be given to the converter in terms of size reduction and cost effectiveness when optimizing efficiency and integration density [3–5]. However, commercially available power inductors are relatively bulky discrete components that preclude the downsizing of the converter [6]. By switching the converter at high frequency and using embedded

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https://doi.org/10.1016/j.mee.2017.12.012
0167-9317/

planar power inductors with a high frequency magnetic material core, significant miniaturization of the inductor and thus of converter is achieved through size reduction and the performance is enhanced through higher inductance density and parasitics suppression. Also, the fabrication process is simplified compared to 3D inductors such as toroidal inductors and more design flexibility is achieved as the inductors can be placed as close as desired to the IC chips. Different technologies have been developed for the fabrication of planar power inductors depending on the used integration approach/substrate and magnetic core material. Planar inductors using ferromagnetic metal alloys (CoZrTa [7–9], FeSi [10], FeNi [11–15]) and nanogranular metal oxides (CoZrO [16–17], CoFeB-SiO2 [18]), built on inorganic substrates such as semiconductor [19–22], ceramic [23–25], magnetic [26–28] and glass [29–30] wafers are not suitable for high frequency IoE power inductors because of their low resistivity which increase eddy losses at high frequency and the heavy clean room installations and complicated micromachining processes involved which increase processing times and cost expensiveness [19–22].Organic substrates/packages such as FR4 and polyimide [31–34] represent a valuable alternative to inorganic technologies because they present the advantage of cheapness, low processing temperatures (<200 °C) and combined fabrication, connection and assembly flexibility with the IC chips on the same package either in a side by side or in a stacked configuration [35–36]. Ferrite materials show high resistivity with a wide selection of permeability from moderate to high values for applications within the range of 100 kHz to 100 MHz [21–22,37–38]. By mixing powders of Ferrite materials with a polymer, ferrite composite magnetic materials [15, 38–39] [19,34] can be deposited using screen printing [30,15,38] for planar power inductors. Screen printing requires only patterned screens for printing which makes the deposition process simple, fast and cost effective compared to microfabrication processes. Very thick layers of magnetic material (hundreds of microns) can be deposited at a much higher deposition rate than sputtering or electroplating. Moreover, the printing is generally done at room temperature and accommodates organic substrates. In this work, we demonstrate a new, low temperature, simple and cheap fabrication process of planar power inductors with two magnetic layers deposited using a cost effective stencil printing process on a very thin, thus lightweight and flexible FR4 organic substrate for high efficiency voltage converter applications in IoE devices. The process allows the fabrication of power inductors with different size and inductance densities in the same batch which can be used in IoE based DC-DC converters with a multitude of switching frequency options based on the inductor self-resonance frequency. The paper is organized as fellows. Section 2 presents the design and modeling procedure of the planar inductors. In Section 3, the fabrication process of the planar inductors is demonstrated. The characterization results of the fabricated inductors are discussed in the last section of the paper and compared to the simulation results.

2. Design and modeling

2.1. Overall IoE architecture

The objective is to design spiral power inductors to be used in a SIP based point of load DC-DC converter using energy harvesting as input power source for an IoE device. Because of the low power levels involved at the input, single or multistage boost regulators are required to power the different analog and digital circuits of the IoE device. Assuming the basic configuration of a boost converter given in Fig. 1, the converter inductor L can be estimated using (1) [40]:

$$L = \frac{V_{IN}.(V_{OUT}-V_{IN})}{\Delta I_L.f_{SW}.V_{OUT}} \quad (1)$$

where V_{IN} is the input voltage, V_{OUT} the desired output voltage, f_{SW} the switching frequency of the converter and ΔI_L the estimated inductor ripple current. By using (1) and assuming a switching frequency between 10 MHz to 30 MHz, an inductor ripple current of 50 mA for a duty cycle value between 0.4 and 0.6, a wide range of inductance values comprised between 170 nH and 750 nH can be selected for the boost converter depending on the output voltage as can be seen in Table 1.

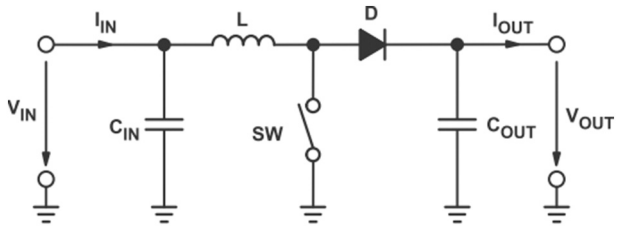

Fig. 1. Basic configuration of a boost converter.

2.2. Inductor geometry

The designed inductors are square planar inductors with two magnetic layers defined on both sides of a two copper layer (35 μm copper thickness for each side) FR4 PWB. The top copper layer is used to define the inductor traces which will be covered with the first magnetic layer. The bottom side copper is used to define trenches underneath the inductor which will be filled with the second magnetic layer. The bottom side copper is also used as a ground plane to reduce the EMI between the inductor and its surrounding. The square shape was chosen for ease of fabrication while the 35 μm copper thickness was selected for DC resistance and inductance tuning. The considered inductor geometry is shown in Fig. 2(a).

The design parameters of the inductors are the outermost length, d, the metal trace width, w, the trace separation s and the number of turns N. The trace separation s is set to be equal to the metal trace width w for each inductor design. SMA pads are included in the design for inductance measurements as well as a simple deembedding structure (microstrip line) with the same width and length as the inductor feedline to eliminate the contribution of the SMA connector and feedline to the inductor inductance.

2.3. Modeling approach

A 3D model of the planar inductor of Fig. 2(b) with two magnetic layers defined on both sides of the inductor was created in the electromagnetic simulator ANSYS HFSS v17. A lumped port simulation was achieved by connecting the top copper traces (port 1) to the bottom (ground) plane (port 2). A current excitation was created through the lumped port to compute the voltage reflection and the corresponding S-parameter (S11). From this S-Parameter, the Z-Parameter (Z11) was extracted and the inductance and Q factor were calculated using (2) and (3). The considered magnetic material is a NiZn ferrite-epoxy composite [41]. The permeability spectrum used for the simulations is shown in Fig. 12(a). The top and bottom magnetic layer thicknesses were set to 200 μm while the design parameters d, w, s and N were varied to get various inductance densities for an inductance range from 200 to 600 nH. The modeling parameters and results are summarized in Table 2 where L_{air} and Q_{air} are the inductance and the quality factor for the air core inductor, L_{mag} and Q_{mag} are the inductance and the quality factor for the magnetic core inductor and f_{SR} is the self-resonant

Table 1
Inductance range selection for the boost converter.

D	ΔI_L (mA)	f_{SW} (MHz)	V_{OUT} (V)	L (nH)
0.4–0.6	50	10–30	1.1–1.5	170–750