Microelectronic Engineering xxx (2017) xxx–xxx

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Research paper

Monolithic technology for silicon nanowires in high-topography architectures

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ARTICLE INFO

Article history:
Received 18 July 2017
Accepted 2 October 2017
Available online xxxx

Keywords:
Silicon nanowire
3D integrated circuit
3D integration
Top-down fabrication
Trench isolation

ABSTRACT

Integration of silicon nanowires (Si NWs) in three-dimensional (3D) devices including integrated circuits (ICs) and microelectromechanical systems (MEMS) leads to enhanced functionality and performance in diverse applications. The immediate challenge to the extensive use of Si NWs in modern electronic devices is their integration with the higher-order architecture. Topography-related limits of integrating Si NWs in the third dimension are addressed in this work. Utilizing a well-tuned combination of etching and protection processes, Si NWs are batch-produced in bulk Si with an extreme trench depth of 40 μm, the highest trench depth obtained in a monolithic fashion within the same Si crystal so far. The implications of the technique for the thick silicon-on-insulator (SOI) technology are investigated. The process is transferred to SOI wafers yielding Si NWs with a critical dimension of 100 nm along with a trench aspect ratio of 50. Electrical measurements verify the prospect of utilizing such suspended Si NWs spanning deep trenches as versatile active components in ICs and MEMS. Introducing a new monolithic approach to obtaining Si NWs and the surrounding higher-order architecture within the same SOI wafer, this work opens up new possibilities for modern sensors and power efficient ICs.

1. Introduction

The integrated circuit (IC) is the primary example of the integration of multiple length scales, where features of the critical dimension (CD) of about 10 nm are ultimately linked to others of characteristic dimensions as large as 100 μm, thereby spanning a four-order-of-magnitude scale difference. The most remarkable aspect of this integration is its batch-compatibility, *i.e.* the achievement of integration using top-down semiconductor manufacturing techniques based on lithography with ultimate registration capabilities [1]. This resulted in the historic downscaling defining the increased IC performance at a reduced cost, which was dubbed "Moore's Law" [2].

Although a similar downscaling took place in micro electromechanical systems (MEMS), the incorporation of multiple length scales has proved to be much more challenging. As in IC, such multiscale systems make the best use of the respective advantages of nano and microscale components as highlighted in new-generation physical sensors [3,4]. For instance, the capability of detecting minute displacements in MEMS thanks to the introduction of highly sensitive nanoscale components lead to ultra-sensitive mechanical biosensors [5] and inertial instruments [6]. Operational enhancement can be obtained through a functional multiscale integration approach [4,7]. Furthermore, with the advent of Internet of Things (IoT) there is a strong motivation for on-chip integration of electromechanical sensors on a massive scale [8]. However, the challenge — similar to IC — is primarily due to the three-dimensional architecture, where involved topographies can be considered extreme. For instance, embedded interconnections and electrical isolation in three-dimensional devices necessitate narrow and deep trench isolation with high-resolution micromachining [9]. Hence, high-resolution lithography alone is not sufficient to secure the success of multiscale integration, where a new approach to processing is needed.

To answer this need for multiscale integration, a wealth of bottom-up approaches was developed over the years [10]. In the majority of integration studies, bottom-up synthesis is followed by

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https://doi.org/10.1016/j.mee.2017.10.001
0167-9317/

field-assisted self-assembly [11]. While self-assembly is a valid tool in applications with less stringent requirements on spatial resolution of integration, it falls short of meeting the demands of the deterministic integration as laid out by semiconductor manufacturing [1]. As an alternative, synthesis sites can be defined via high-resolution lithography, a hybrid approach linking self-assembly with top-down fabrication, where integration is generally limited to out-of-plane growth [10]. Pick-and-place assembly is yet another top-down approach for manipulating and placing synthesis products. Due to the high level of control it provides, pick-and-place assembly is a highly preferred tool in pilot studies, while the assembly time is the major drawback. For example, compared to printed wiring board assembly in terms of the number of assembled parts, pick-and-place assembly via scanning probe microscopy is three orders of magnitude slower [12]. In this context there is a certain lack of sound technologies with the capability of bridging significant scale gaps in a batch-compatible fashion. Hence, innovative approaches based on semiconductor manufacturing are in high demand [1].

One such technique was recently demonstrated for the monolithic incorporation of silicon nanowires (Si NWs) in bulk Si in the presence of an etch depth of 10 μm [13]. The approach is based on high-resolution lithography and deep etching technology and resembles the single-crystal-silicon reactive etching and metallization (SCREAM) process [14]. A nanoscale protrusion created on the substrate surface through a shallow reactive ion etching (RIE) step is encapsulated against the detrimental effects of the subsequent deep reactive ion etching (DRIE). The isotropic component of DRIE creates a sufficiently deep undercut and thereby releases the nanoscale protrusion in the form of a Si NW. Although the fragile, encapsulated Si NW remains unprotected along its newly formed bottom surface, it survives the deep etch. As a result, the process successfully spans a two-order-of-magnitude scale gap. Although this technique was recently utilized to introduce new-generation piezoresistive sensors [15] and mechanical testing platforms [16], ultimate limits of such monolithic integration remain to be addressed for 3D devices with high-topography architectures.

The present work inquires further into the deep etch limit provided by this technology. For this purpose, a single suspended Si NW is integrated into a double-gated architecture. Fabrication approach is explained in detail. Challenges associated with the structural evolution of the Si NW as a function of the etch depth are highlighted through a transmission electron microscope (TEM) study. An extreme etch depth of 40 μm is achieved for a Si NW of a CD of 80 nm in bulk Si. The successful combination of high-resolution lithography and deep trench isolation is then repeated on a thick SOI. This time the maximum trench aspect ratio (TAR) of 50 with a 200-nm trench gap is demonstrated. In addition to the etch depth of 40 μm achieved in bulk Si, this figure of TAR also sets an upper limit to match for future integration studies. Associated challenges of transferring the technology to SOI are discussed. The work is concluded with a discussion on the maximum achievable TAR.

2. Fabrication approach

The incorporation of a NW within a higher-order architecture such as MEMS or CMOS with a three-order-of-magnitude scale difference constitutes an active field of study, as NWs are shown to impart significant improvements in the operation of electronic and electromechanical systems [17–20]. Although such a quest for a monolithic approach is critical for the technological relevance and the transition from pilot systems to applications, associated efforts are marred by compatibility challenges. The foremost challenge is concerned with the protection of this miniature component against free fluorine radicals during the deep etch stage. In the present work, the limits of such a nanoscale protection technology are investigated using NW bridges spanning thick Si islands. The initial demonstration of the technology was presented with an etch depth of 10 μm in bulk Si [13]. The question of how deep one can etch the surrounding architecture while NWs retaining their structural integrity remains yet to be addressed.

The associated process flow is depicted in Fig. 1. Patterning of the NW is carried out by e-beam lithography using a 600-nm-thick HSQ 21% (hydrogen silsesquioxane) resist on a p-type, <100> Si wafer of 100-mm diameter, 525-μm thickness and a resistivity of 5 Ωcm (Fig. 1a). HSQ is spin-coated at 4000 rpm after a wafer surface activation in Tepla Gigabatch oxygen plasma system with a power of 600 W and O_2 flow rate of 400 sccm for 5 min. e-Beam lithography is executed in Vistec EBPG5000 system with a beam energy of 100 keV. e-Beam dose calibration is carried out to define the proper dose for the optimum e-beam size. NW pattern is defined along <110> crystal orientation with a 2 nA beam spot and a dose of 2500 μC cm^{-2}. Exposure is followed by development in tetramethylammonium hydroxide (TMAH) 25% for 2 min. Chlorine RIE in a STS multiplex inductively coupled plasma (ICP) etcher is utilized for the anisotropic silicon thin film etching. RIE is carried out for 45 s for the

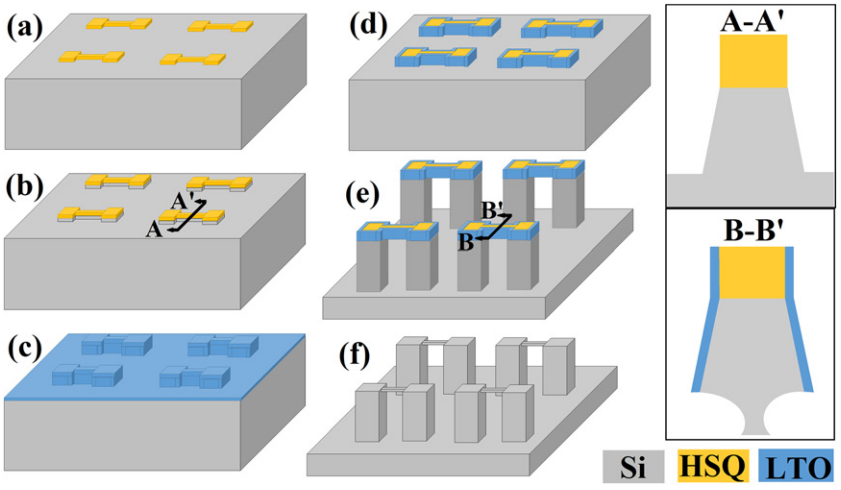

Fig. 1. Process flow for the fabrication of suspended Si NWs, (a) e-beam lithography, (b) reactive ion etching (shallow etch), (c) low-temperature oxide coating, (d) directional oxide etching, (e) deep reactive ion etching, (f) removal of all protective layers. The sketch is not drawn to scale. Si NW has a CD of 80 nm, whereas the maximum trench depth achieved is 40 μm.

Please cite this article as: M. Esfahani et al., Monolithic technology for silicon nanowires in high-topography architectures , Microelectronic Engineering (2017), https://doi.org/10.1016/j.mee.2017.10.001