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Advances in fabrication of X-ray waveguides

Sarah Hoffmann-Urlaub *, Philipp Höhne, Mike Kanbach, Tim Salditt

Institut für Röntgenphysik, Universität Göttingen, Friedrich-Hund Platz 1, 37077 Göttingen, Germany

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ABSTRACT

This paper reports on the fabrication of X-ray waveguides, manufactured by e-beam lithography, reactive ion etching and wafer bonding techniques. By combination of these processing steps, long empty (air) channels with cross-sections in the range of 10 to 100 nm are obtained, forming a guiding layer, surrounded by a solid state cladding. Aside from silicon, we present also waveguide channels fabricated in germanium and quartz. The improved fabrication protocols lead to significantly enhanced exit flux for imaging applications. Finally, we address not only straight channels, but a large variety of various geometries, as required for different applications.

1. Introduction

While waveguide (WG) optics is ubiquitous in the visible and infrared spectral range, it is still much less developed in the X-ray regime, despite some encouraging initial work on planar X-ray WGs [1–8]. This is for a good reason. The guiding channel cross-sections in the range of 10 to 100 nm and the required length to reach well defined propagation regimes, are extremely challenging in view of fabrication. As in other X-ray focusing optics, such as Fresnel zone plates [9–11] or compact refractive lenses [12–14], the combination of small wavelength and vanishing differences in the index of refraction $n \approx 1$, leads to areas and aspect ratios which are very different from their counterparts in visible light optics. Ideally, an X-ray WG consist of an empty (air filled) channel, embedded in a moderately absorbing material (cladding), with the entrance (front) and exit sides of the channel left open for coupling and decoupling of guided beam. Hence, an X-ray WG essentially corresponds to a long empty fiber defined in a solid body. For example, typical hard X-ray photon energies ($E_{ph} > 10$ keV) require a significant propagation length in the channel to sufficiently block radiative modes in the cladding. The aspect ratios are hence in the range of $1{:}10^4 - 10^5$. The long channel length results in multiple internal reflections increasing the probability of the X-rays to be scattered by defects or side wall roughness [15]. To avoid leakage and over-illumination also the cladding has to be sufficiently thick, resulting in 'buried' channels. Recent progress in fabrication has helped to meet these challenges [16], and have enabled promising applications in nanoscale holographic X-ray imaging [17,18]. The experiments took advantages of the optical properties of X-ray WGs in confining and filtering synchrotron radiation and of the quasi-point source illumination which they can provide for cone beam holographic imaging. Nano-manufacturing of WGs combines different fabrication steps and techniques, namely e-beam lithography (EBL), reactive ion etching and wafer bonding. As a result of the high flexibility of these process steps, a multitude of channel geometries is feasible. In analogy to lab-on-a-chip approaches, this could become a strategy for X-ray optics on a chip [19]. In practice, such integrated X-ray nano-optics will be limited to a large extent by fabrication issues. Since the guiding effect of the WGs is based on total reflection, smooth channel boundaries are required. To this end, a precisely controlled fabrication process is needed. The optimized protocols as presented here now offer better control of the channel cross-section, and enhanced smoothness of the side walls, leading in turn to better X-ray optical performance. Apart from straight WGs [16], we also address fabrication of WGs with a tapered geometry for beam concentration [20], as well as curved channels and WG arrays. Finally, we broaden the range of materials, beyond the channels in Si presented in [16], also to quartz (SiO_2) and Ge. The latter will be particularly useful for high photon energies.

2. Experimental methods

Wafers of Si (University Wafer), Ge (MaTeck) and SiO_2 (Quartz Unlimited LLC) each with a diameter of 4 in. were covered by an e-beam resist (ARP 679.04, Allresist), consisting of a poly-methyl methacrylate (PMMA) solution. The resist was spin coated (Optispin SB20, Sister Semiconductor Equipment) onto the wafer at 2000 rpm for 70 s, followed by a post baking step (180 °C for 90 s). In the case of SiO_2, an additional resist (SX AR-PC 5000/90.2, Allresist) was used to enable EBL (e-LiNE, Raith) on the insulating substrate. After spin-coating at

* Corresponding author.
E-mail address: shoffma3@gwdg.de (S. Hoffmann-Urlaub).

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2000 rpm for 60 s the associated baking step of 120 s at 90 °C was performed. Arrays of lines and curves were exposed by EBL. For lines wider than 300 nm an area dose of 200 C/cm^2 and for smaller ones 600 C/cm^2 was chosen. Single pixel lines were exposed with 3000 pC/cm. The SiO_2 was plunged into deionized water for 60 s to clean the sample from the conductive resist. To remove the illuminated resist from all samples, a development procedure with a mixture of Methyl isobutyl ketone and 2-Propanol (IPA) with a ratio of 1:3 at 0 °C for 30 s was carried out [21]. The process was stopped by immersing the sample in pure IPA at room temperature for 30 s. Afterwards the pattern was transferred to the wafer by reactive ion etching (PlasmaLab, Oxford) employing CHF_3 for sidewall passivation [22]. The details for the subsequent fabrication steps are listed in Table 1.

The etching step was performed according to the parameters listed in Table 1. Afterwards, the resist was removed either using an RCA solution for 15 min at a temperature of 65 °C or HCl at room temperature for 10 min. Each of the structured wafers was manually covered with a second wafer of the same material. Instantly, the wafers are kept together by van-der-Waals bonds which are transformed to covalent bonds during the wafer bonding process [24] in an oven (L 3/11/P330, Nabertherm) under a N_2 atmosphere (flow rate 50 l/h). Since the melting point of Ge (937 °C) is lower than for Si (1412 °C) [25], a decreased bonding temperature T_b was chosen accordingly. At higher temperatures, channels with a size in the range of 100 × 100 nm^2 were closed due to diffusion processes, which was also the case for SiO_2. The chips were cut to the chosen geometry (DAD320, Disco), leaving the entrance and exit sides of the channels open. For Si, an infrared camera (XEVA XS Base, Xenics) enabled the inspection of the embedded structures from a top view perspective. For inspection of the SiO_2 channels, a fluorescence microscope (Axio Observer Z1, Zeiss) was used, after filling the channels by capillary suction with an aqueous solution of fluorescein (Uranin, $C_{20}H_{10}Na_2O_5$ at 100 mM [26]).

The manufacturing sequence described above corresponds to the optimized protocol. The main difference to the previously published protocol for Si WG fabrication [16] is in replacing the formerly used PMMA resist (A2, MicroChem) by a PMMA resist of higher viscosity, which in turn entails small modifications of the parameters in the following processing steps (spin-coating, e-beam lithography, etching), as described above. The main advantage of this replacement is a higher resist film thickness. The previous protocol enabled a film thickness of only 100 nm, as obtained for spin-coating at 2000 rpm for 60 s. This limited the etching time to 70 s, before the resist was completely consumed. The improved protocol now enables a larger range of etching times and correspondingly larger range of etching depths, as tabulated above. A second important difference is that we now refrain from a cleaning step, in which the wafers were exposed to an O_2 plasma up to 30 min. This was intended to achieve a hydrophilic surface in order to enhance bonding strength. However, the oxygen gassed out in the oven resulting in unwanted bubbles at the bonding interface, as further detailed below.

Table 1
Processing parameters for etching, cleaning and wafer bonding steps for the different materials.

Wafer	Etching			Cleaning procedure	Bonding	
	Gases	t_e	Depth		T_b	t_b
	[sccm]	[s]	[nm]		[°C]	[h]
Si	SF_6:CHF_3/40:10	160	400	RCA[a]	1000	4
Ge	SF_6:CHF_3/40:10	160	320	HCl	650	4
Quartz	CF_4:CHF_3/20:30	590	160	DI-H_2O/RCA	550	12

[a] A mixture of ammonia (32%), hydrogen peroxide (30%) and deionized water (1:1:5) [23].

3. Results and discussion

To characterize the WGs, light microscopy (LM), scanning electron microscopy (SEM), infrared (IR) microscopy and finally X-ray nano-optical testing were performed. Several Si channels are depicted in Fig. 1 to illustrate typical geometries.

Fig. 1 (a) shows a LM image of a typical X-ray WG array, both with large channels for alignment and small ones, which confine and guide the beam in both lateral axis. The Si is covered with the e-beam resist which also serves as a mask during the etching process. Channels broader than 300 nm are silhouetted against the homogeneous background as bright lines, while the narrower ones appear darker.

In (b,c) IR transmission images of bonded wafer-pairs are depicted. Round or elliptically shaped dark spots accompanied by interference fringes are observed, indicative of voids between the two wafers [27]. These unbonded regions or embedded gas reservoirs can be caused by trapped gas, imperfections on the wafers surface or by particles. In this work, the dominating effect was gas bubbles originating from molecules desorbing from the wafers during annealing. Usually the gas consists of water or hydrocarbons [28], which at high temperature can only be dissolved in small amounts in the bulk Si or the interfacial oxide layer. Micro-defects at the surface then serve as nucleation sites for bubble formation [29], as is frequently observed after oxygen plasma treatment [30]. For this reason, plasma cleaned wafers are often found to be highly covered with voids (b), affecting the local bonding quality. Substituting the plasma cleaning by an RCA bath decreases the number of (small) bubbles significantly, while hardly reducing the bonding strength between the wafers [31]. Contamination is identified as the dominant mechanism of generating large bubbles at the RCA cleaned wafers, since micron-sized particles induce voids with a diameter up to several centimeters. Therefore, in (c) mainly bubbles with diameters ≥ 0.5 cm are observed, which can in many cases be removed

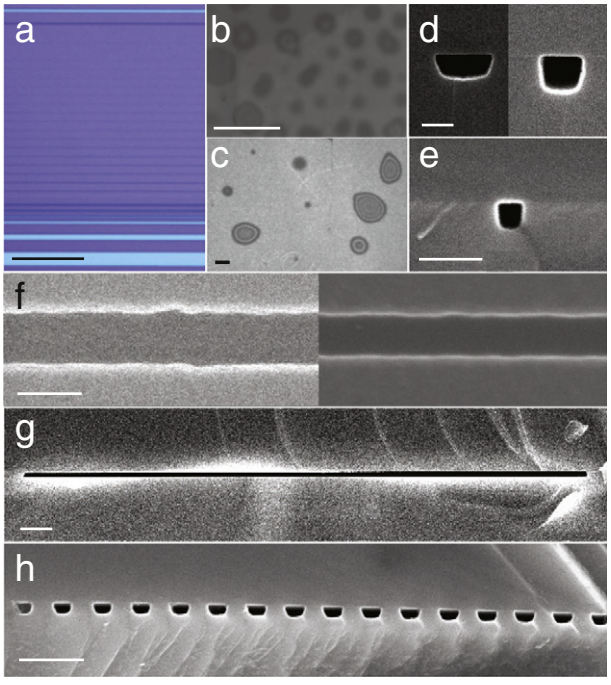

Fig. 1. Structured Si wafers. (a) LM top view of a WG chip after development, before etching. Scale bar denotes 100 m. (b,c) IR images of bubbles between bonded wafers, processed according to the old (b) and new (c) protocol. Scale bars denote 5 mm. (d,e) SEM images of the exit planes of final WG channels and (f) a top view of an unbonded (open) channel. In (d,f) the left part shows the old protocol and the right the new one. Scale bars denote 100 nm. (g,h) SEM images of exit planes of final channels, showing (g) a channel with a broad entrance (for beam compression by tapering), and (h) an array of WG channels. Scale bars denote 1 µm.