



Post-annealing processes to improve inhomogeneity of Schottky barrier height in Ti/Al 4H-SiC Schottky barrier diode



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ARTICLE INFO

Article history:

Received 29 September 2015

Received in revised form 3 December 2015

Accepted 15 January 2016

Available online 16 January 2016

Keywords:

4H-SiC Schottky barrier diode

Post-annealing

Schottky barrier height

Transformation

Diffusion

Inhomogeneity

ABSTRACT

To improve the high resistance and low breakdown voltage (BV) of a 4H-SiC Schottky barrier diode (SBD), the metal annealing process is conventionally used; this process stabilizes the Schottky barrier height (SBH). In this paper, we apply a post-metal annealing process to 4H-SiC Ti-SBD chips and verify the effect of the changes on electrical characteristics based on the post-annealing process. The results of experiments show that the condition of 873 K/30 min annealing created a stable SBH and a low value of on-resistance (R_{on}), which improved inhomogeneity. Based on the results of EDX and TEM analysis, the cause of improved SBH at the condition of 30 min was attributed to the generation of $TiSi_x$ (which has a higher SBH than Ti). On the other hand, the improved value of R_{on} at the condition of 30 min was attributed to the change to γ -phase Ti_3Al (which has a low resistance because diffused Al is present) caused by proper annealing. However, when more heat is applied in the cases of 773 K/60 min and 873 K/60 min, R_{on} increased and the SBH decreased. The results of EDX and TEM analysis showed that the low SBH was caused by Al spiking, which created an Al Schottky junction with a lower SBH than that of the Ti Schottky junction. Higher R_{on} resulted from the change to α -TiAl phase at the Al–Ti interface layer because of excessive diffusion of Ti and Al, which is due to the overly applied heat. From the results produced by this work, we can enhance the Al–Ti 4H-SiC SBD electrical characteristics by applying a suitable post-annealing process.

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1. Introduction

A silicon carbide Schottky barrier diode (SiC SBD) is a superior power device in terms of fast switching and low built-in voltage. However, the SiC SBD also has a high on-resistance and a high leakage current compared to a silicon *pn* diode at the same forward voltage. The forward and reverse characteristics of the SiC SBD were determined using the thermionic emission model and the Schottky barrier height (SBH) [1]. In practice, the Schottky metal determines the SBH, which, in turn determines the *I*–*V* characteristics. Titanium (Ti) is traditionally used as a Schottky metal as it has a low SBH, resulting in a low forward voltage drop. However, undesirable *I*–*V* characteristics often appear in Ti–SiC SBDs, which are affected by an incomplete SBH resulting from interface states, residual processing-induced contamination, inhomogeneous doping, and crystal orientation [2]. This incomplete SBH causes increasing reverse leakage current and subthreshold current; many treatments have been researched to improve contact quality [3]. Among them,

thermal treatment is widely used to obtain a stable SBH and to decrease resistance at the interface between the silicon carbide and the Schottky metal [3–5]. However, despite the excellent effects of thermal treatment, few studies regarding the annealing condition and its effects have been published.

In this paper, we have applied post-metal annealing to 4H-SiC Ti-SBD chips and verified its effects on the electrical characteristics.

2. Experiments

2.1. Fabrication and experiments

As shown in Fig. 1, the samples were fabricated at a chip size of 1 mm² on a 4-inch 4H-SiC wafer with a 11.5- μ m *N*-epitaxial layer doped at 1×10^{16} cm^{−3} and a 338.5- μ m substrate layer doped at 2×10^{18} cm^{−3} from Cree Inc. Samples were processed using Ti (2000 Å), Al (4- μ m), and nitride (Si₃N₄) passivation. The Ti and Al were deposited using sputtering after sacrificial oxidation and surface cleaning with buffered oxide etch solution.

A nitride passivation layer was deposited using CVD. Although we designed a 10 [A]/600 [V] 4H-SiC SBD, we observed failure of chips in their forward currents (I_F) under 1 A at a forward voltage of (V_F)

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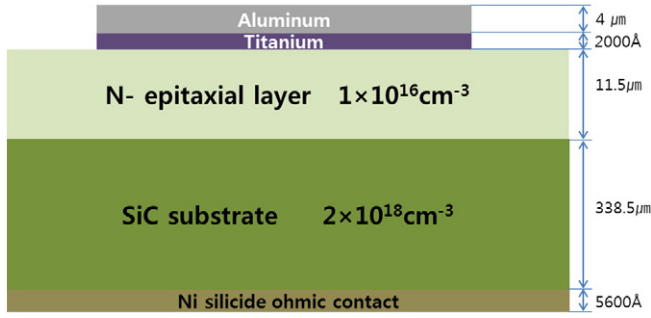


Fig. 1. Structure of Al–Ti 4H–SiC Schottky barrier diode.

1.5 V. In Fig. 2, SBH inhomogeneity is seen in the forward characteristics graph consisting of low SBH (LSBH) and high SBH (HSBH) curves [4]. Reviewing the process history, the Schottky metal annealing step process time was not long enough, because of the facility event.

Based on review, the post-annealing process experiments were planned to address the failures, as with previous research which improved electrical characteristics using thermal treatment [3–5]. With reference to the earlier studies of thermal treatment and SBH inhomogeneity, experimental conditions included 773-K or 873-K treatment during a 30-minute or 60-minute period and a metal annealing tube (in N₂ gas at 1.0×10^{-3} Torr) [3–5]. The temperature conditions of the experiments were determined based on the conventional metal annealing condition (673 K/30 min) of Ti Schottky metal and Al.

2.2. Experimental electrical characteristics

The experimental electrical characteristics of experimental chips are shown in Fig. 3.

The differences in J_0 , J_1 , and J_2 (conditions before annealing, 773 K/30 min, and 873 K/30 min, respectively) show a decreasing subthreshold current density under an applied turn-on voltage. The forward current densities of J_1 and J_2 are greater than that of J_0 .

Conversely, both current density and subthreshold current density decreased in J_3 (condition of 773 K/60 min). In J_4 (condition of 773 K/60 min), the subthreshold current density increased relative to that of J_3 .

Even in the case of reverse bias, J_1 and J_2 show improved leakage relative to that of J_0 . In contrast, J_3 and J_4 become worse than J_0 ; i.e., leakage current densities increased.

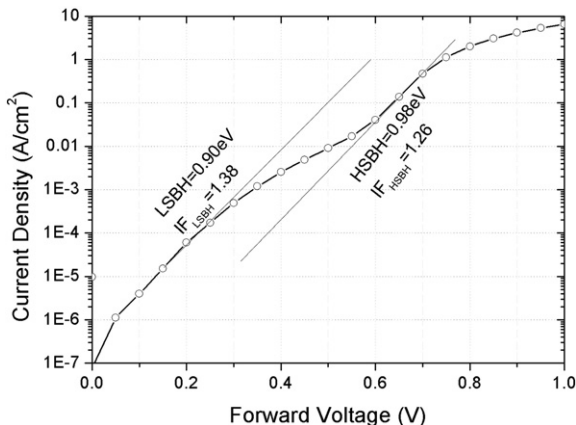
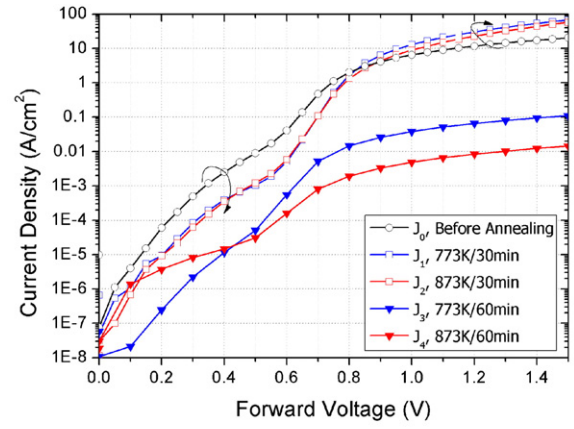
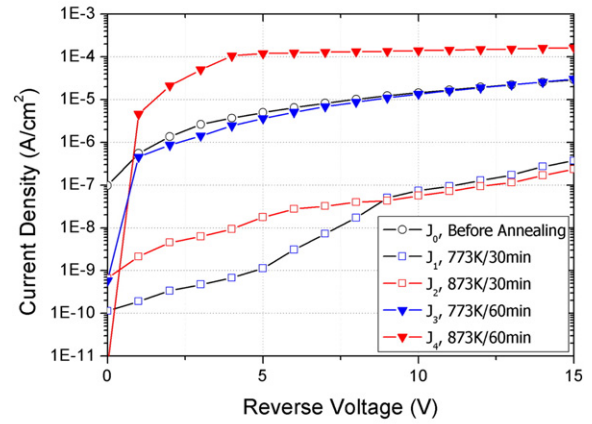


Fig. 2. Forward characteristics of 4H–SiC Schottky barrier diode with LSBH and HSBH.



(a) Forward characteristics



(b) Reverse characteristics

Fig. 3. Measured I – V curves for different annealing conditions.

3. Analysis

3.1. Electrical analysis

In the 4H–SiC SBD, the electric characteristics are usually explained using thermionic emission–diffusion theory (TED), which includes the resistive voltage drop, as in Eq. (1):

$$I = I_s \left[\exp \left(\frac{q(V_F - R_{on}I)}{nkT} \right) - 1 \right] \quad (1)$$

in which the saturation current I_s is defined by Eq. (2), where I_s is the same as the reverse leakage current [1].

$$I_s = AA^*T^2 \exp \left(-\frac{q\phi_B}{kT} \right) = -I_{reverse/leakage} \quad (2)$$

In the above equations, A^* is the effective Richardson's constant, V_F is the applied forward bias, n is the ideality factor, R_{on} is the specific on-resistance, and k is the Boltzmann constant.

Table 1

Extracted SBH (ϕ_B), ideality factor (n), and specific on-resistance (R_{on}).

Annealing condition	ϕ_B [eV]	n	R_{on} [$m\Omega \cdot cm^2$]
Before annealing	0.96	1.29	3.57
773 K/30 min	1.07	1.19	1.89
873 K/30 min	1.08	1.16	1.26
773 K/60 min	0.93	1.37	6.68
873 K/60 min	0.85	1.86	48.49

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