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Fabrication of high-resolution, self-aligned palladium electrodes

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ABSTRACT

Here, a fabrication approach is presented, which allows for the patterning of vertically displaced, high density and high resolution palladium electrodes in a single processing step. A top down method, namely ion milling, was used to transfer the e-beam lithography pattern into the palladium. Hereby hydrogen silsesquioxane (HSQ) was employed as a hard mask. Other than the conventionally used lift-off based approach, this method does not restrict the line height to spacing ratio and therefore permits the fabrication of very densely spaced electrodes. Specifically, electrodes with as little as 25 nm spacing were obtained, although only lines with spacings of 80 nm or more were electrically isolated without any further processing. By adjusting the tilting angle and the HSQ to Pd thickness the cross-sectional profile can be controlled and varied from triangular (30° side-wall slope at 10° tilt) to rectangular (30° tilt). This can be used to its advantage in order to reduce the parasitic capacitance of adjacent lines for a given pitch. Additionally, a proximity effect was observed as the decrease of spacing of electrodes was correlated with an increase in side-wall verticality. In summary, we have demonstrated a robust process to pattern perfectly aligned electrodes on complex topographical substrates. The here presented method is characterized by a high degree of scalability and also high flexibility in terms of materials selection.

1. Introduction

Palladium (Pd) is known to form excellent contacts with low-dimensional carbon materials, in particular with single-walled carbon nanotubes (SWNTs). Specifically, favorable wetting properties and a high on-off current ratio have previously been observed [1]. Simultaneously palladium is difficult to chemically dry etch [2,3], therefore the choice of fabrication methods for nanostructures is primarily limited to lift-off and physical etching.

Here, we present an ion milling based approach to pattern densely spaced high-resolution source, drain and gate electrodes in a single step on a pre-patterned substrate. Unlike lift-off based processes this approach does not limit the spacing between adjacent electrodes with respect to the desired line height.

These vertically displaced electrodes can then later be used to transfer a carbon nanotube (CNT) from a separate growth substrate on top, in order to create functional devices [4–6].

For suspended CNT devices in field-effect-transistor (FET) architecture (see Fig. 1.a) scaling down the gate dimensions and electrode spacings allows for the fabrication of ultra-short channel devices, but also enables the packing of multiple gate electrodes between the source and drain (see Fig. 1.b). These structures can be used for local actuation and sensing [5]. Hereby quantum-effects can be studied [5,7,8] and also, in case of resonant devices, mode coupling [9,10] can be investigated. Using a one-step process in comparison to a conventional 2-step process means that the exact relative location of the electrodes is well defined (see Fig. 1.c). This permits a further decrease in spacing between adjacent electrodes.

2. Materials and methods

A layer stack of 200 nm plasma-enhanced chemical vapor deposited SiN_x (PECVD, at 300 °C, 120 sccm SiH_4 + 1000 sccm N_2), 2 nm atomic layer deposited Al_2O_3 (ALD, at 250 °C), 100 nm PECVD SiN_x was precipitated onto a Si (100) wafer and annealed in a rapid thermal annealing system (AS One 150) at 850 °C. This results in an increased wet-etch resistance of the nitride layers [11] and the recrystallization of the alumina layer. For ALD alumina the transition to α-alumina has been observed at temperatures as low as 750 °C [12]. In comparison to amorphous alumina, α-alumina is compatible to hydrofluoric acid (HF) as well as vapor HF [3,13]. This is required here for a release step of suspended Si-structures at a later stage. This layer stack was patterned (see Fig. 1.d) using a negative e-beam resist (AR-N 7520.18, 400 nm, e-beam tool: Vistec EBPG 5200+ at 100 kV). A CHF_3 based RIE process was used to pattern the SiN_x layer with the alumina as an etch stop.

Onto this pre-patterned substrate 2 nm chromium and 73 nm palladium were evaporated. Next, a 20 nm layer of SiO_2 was deposited using a PECVD process (300 °C, 150 sccm SiH_4 + 710 sccm N_2O) to improve the surface adhesion of hydrogen silsesquioxane (HSQ, XR-1541.006), which was used as the high-resolution e-beam resist. After e-beam writing and development (with AZ351B) the layer was ion milled (Oxford Ionfab 300, ion currents of 250 to 500 mA, acceleration voltage of 350–500 V, at a processing pressure of $7°10^{-5}$ Torr and a platen

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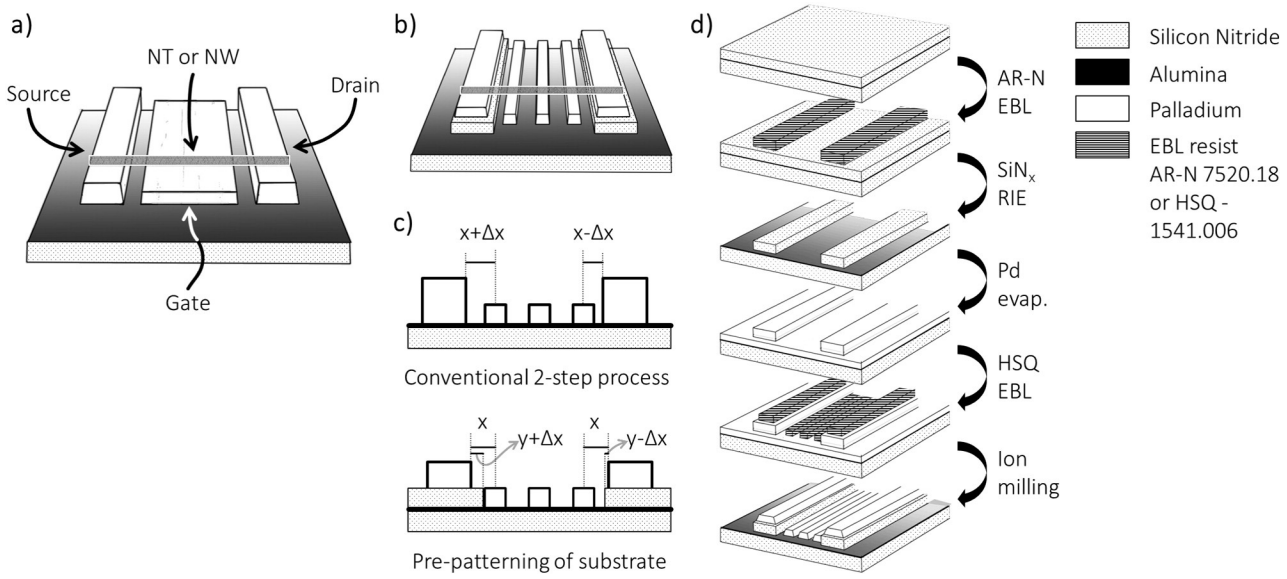

Fig. 1. a) A typical nanoresonator design. b) CNT on a multi-gate structure. c) By choosing to pattern electrodes on a pre-patterned substrate rather than using a conventional two-step process the misalignment is shifted to between the electrodes and substrate rather than the electrodes themselves. d) Fabrication steps for the here demonstrated structures.

temperature of 5 °C), while using secondary ion mass spectroscopy (SIMS) to detect when the end of the process was reached. Palladium is highly chemically stable. In particular in fluorine based plasmas a Pd-F film evolves, which is even more chemically stable than bulk Pd [2]. Chemical etching of palladium in chlorine plasmas is as of yet unreported. As a result it can only be effectively etched by sputtering [3]. HSQ was chosen for ion milling due to its low etch rate in comparison to Pd, its high resolution and low line roughness [3,14].

The structures were analyzed electrically (resistance and leakage current measurements) and by scanning electron microscopy (SEM).

3. Results and discussion

The primary focus here was on the quality of the pattern transfer, the limitations in terms of half-pitch relative to the electrode height and width and the overall constraints put on the process by the overlay mismatch of the e-beam writing.

For the pre-patterning of the insulating layer precise control of the step height between the gate electrode and the source/drain electrode level was essential. Therefore a 2 nm Al_2O_3 etch stop was employed. 2 nm of alumina proved to be enough to withstand over-etching (etch rate of alumina 0.95 nm/min, silicon nitride: 30.5 nm/min). Slight over-etching was necessary in order to compensate for micro- or macro-loading effects [15].

After palladium deposition a smooth step coverage was observed within the transition region, which is of importance in order to be able to spin the HSQ uniformly for the following processing steps.

For the pattern transfer of the HSQ lines into the palladium layer, it was observed that a high degree of profile control could be obtained by adjusting the ratio of palladium to HSQ thickness and choosing the tilting angle accordingly. The theoretical etch rate of palladium to HSQ is around 1:1 (Pd etch rate ~ 20 nm/min at 250 mA, 10° tilt β, see Fig. 2) [3]. In reality, an etch rate much closer to 1:2 was observed, which is due to the faster propagation of the etch-front in the facets that develop rather than in perpendicular direction to the surface.

The etching of the HSQ hard mask and the palladium follow different trends primarily because their etch products display significantly different levels of redeposition. HSQ is chemically identical to polycrystalline SiO_2, with some structural defects and residual Si—H bonds. For most materials the sputter yield, while neglecting any redeposition, follows a similar trend with a maximum sputter yield at approximately 75° (relative to the vertical) [16]. This is a result of only the re-sputtered atoms close to the surface in the interaction volume being able to escape. Therefore at high tilting angles (β) the highest degree of material

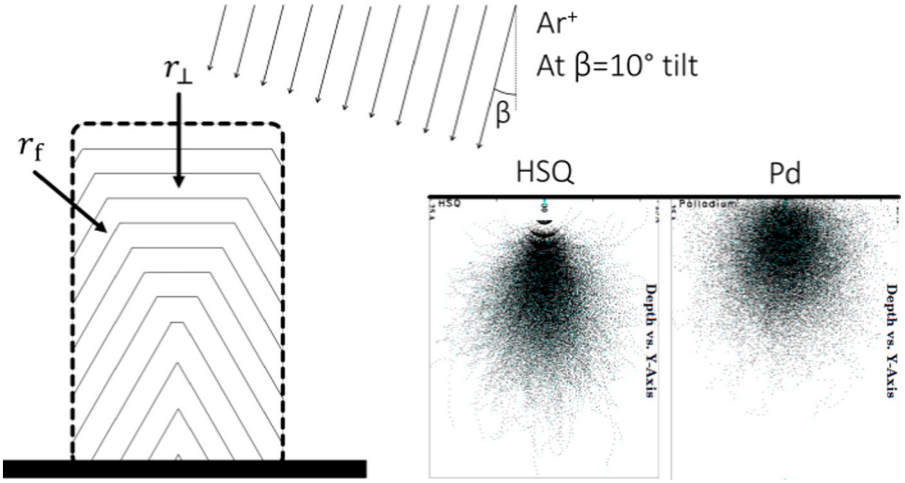

Fig. 2. Facet development due to angle dependent sputter yield ($r_f > r_\perp$) during etching of HSQ and TRIM simulations of the interaction volume of 500 eV Ar ions with HSQ and Pd.