Microelectronic Engineering 147 (2015) 344–348

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

III–V nanowires for logics and beyond

Lars-Erik Wernersson

Electrical and Information Technology, Lund University, Box 118, S-221 00 Lund, Sweden

ARTICLE INFO

Article history:
Received 4 March 2015
Received in revised form 21 April 2015
Accepted 22 April 2015
Available online 30 April 2015

Keywords:
III–V MOSFETs
Nanowires
InGaAs
InAs

ABSTRACT

III–V MOSFETs are currently being considered for digital applications, whereas the option to develop the technology for RF-applications is less often discussed. The quality of the semiconductor/high-*k* interface and the presence of border traps within the high-*k* film plays an important role in both types of transistors, but given the different sets of transistor metrics, their influence is different although correlated. The high-*k* technology developed for digital transistors will be applicable also to RF-transistors, while special attention needs to be given the frequency dispersion of the transconductance and the low-frequency noise. Following the natural transistor evolution, III–V nanowires need to be used to maintain electrostatic control at scaled gate lengths. Finally, examples of heterostructure design and circuit implementation are given describing status in the field.

1. Introduction

III–V Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) are currently being developed to extend the roadmap for the CMOS scaling [1]. The advantageous transport properties of the III–V materials will allow for a higher drive current at moderate drive voltages as compared to Si-based technologies. Key technological steps like gate-last processes using dummy gates, fabricated for instance from hydrogen silsesquioxane (HSQ) [2], combined with epitaxial regrowth techniques have enabled devices with advantageous performance. Although substantial progress has been made towards the implementation of logic devices, several challenges still exist related to the reduction of the defect density at the III–V/high-*k* interface and the reduction of the border trap state density within the high-*k* film. The co-integration of n- and p-type devices and their integration on large scale Si wafers are further issues. From the transistor evolution, it is clear that future technology nodes will use non-planar geometries to maintain electrostatic integrity as we scale the gate length [3]. Lateral III–V FinFETs or nanowire FET will be considered as a first step, whereas vertical transistor architectures may be considered later to increase the package density and to use 3D contact schemes [3]. It is hence essential to consider not only planar transistor architectures, as nanowire-based implementations will be required to enable future nodes.

In an alternative perspective, it has recently been pointed out that the III–V MOSFETs over the last few years have shown a dramatic increase in the transconductance [3], what is one of the main on-state performance metric. Currently, the best MOSFETs show comparable, or even higher, transconductance as compared to high-performance III–V High Electron Mobility Transistors (HEMTs) and they also show advantageous low on-resistance. The compact MOSFET architecture with raised source/drain contacts located in the direct vicinity of the gate is a key factor for performance. Given these demonstrated benefits, it is intriguing to address not only logic applications, but also RF-application areas. In this scenario, it is essential to study how the dielectric properties will affect the RF-device metrics and what material combination will provide the best performance.

In this paper, we outline the essential transistor metrics used to characterize digital- and RF-transistors and we describe how both sets of metrics are connected to the properties of the dielectric film and the interface properties. Status in the field of RF-MOSFETs is discussed and data demonstrating how III–V heterostructure technology may be used to improve transistor performance, such as off-state leakage and breakdown, is presented. Finally, we show a different III–V MOSFET application in terms of a switch, used to generate pulsed RF-signals suitable for communication and radar.

2. III–V n-MOSFETs for logics, RF-devices, and switches

Studies on Metal-Oxide-Semiconductor (MOS) capacitors are often used to determine the quality of the dielectric layers and their interface towards the semiconductor. The data reveal the possibility to move the Fermi level within the band structure and the defect states as well as the detailed dynamic carrier response related to trapping/detrapping at interface states located within the semiconductor band gap as well as from states originating

E-mail address: lars-erik.wernersson@eit.lth.se

http://dx.doi.org/10.1016/j.mee.2015.04.122
0167-9317/

deeper into the dielectric layer, see for instance [4,5]. Such studies are often complemented by structural analysis of the chemical composition at the interface and modeling of the defect state location [6–9]. Fig. 1 shows a typical data set for n-type devices where the frequency and voltage dependence of the depletion capacitance quantifies the magnitude and energy position of defect states within the band gap. One alternative and direct method to evaluate the III–V MOS materials quality are the ability to move the Fermi-level within the band structure is to measure the complete transistor characteristics including the off-state subthreshold current and the on-state drive current. Here, the inverse subthreshold slope may be used to quantify the interface state density within the band gap, D_{it}, whereas the on-state drive current relates to the channel transport properties as well as the Fermi-level pinning and the interface state density in the conduction band [10,11]. As pointed out in Fig. 1, these measurements are related and provide complementary information about the quality of the high-k material and the interface properties.

2.1. Logics

In digital applications, the transistor off-state performance is essential as we need to meet the leakage current targets defined in the road map. A degraded subthreshold slope will reduce the on-state drive current for a given logic swing, as more bias will be required to reach the threshold voltage. Much focus has hence been given to the characterization and improvement in interface state density, D_{it}, and the relation between the surface chemistry and the subthreshold slope with the goal to obtain competitive values [4–9].

InGaAs is widely considered as the best option channel material for III–V n-MOSFETs due to the advantageous electron mobility

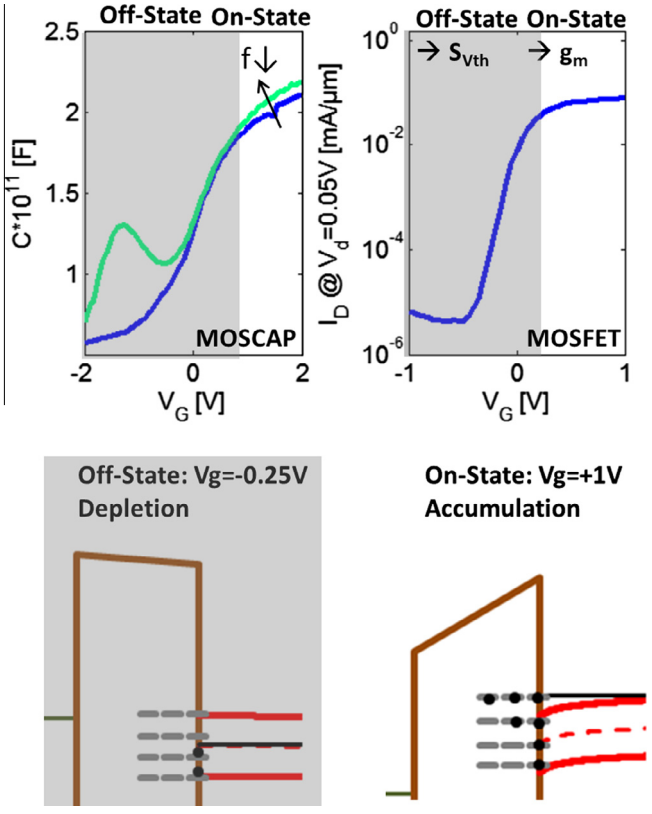

Fig. 1. Above: representative measured data for MOS capacitor (left) and MOSFET (right) with the corresponding off-state and on-state. Below: schematic illustration of the III–V/high-k band structure with carrier trapping at the off-state/depletion (left) and on-state/accumulation (right).

coupled with an adequate band gap that will suppress tunneling transport across the band gap. Transistors with inverse subthreshold slopes of 85 mV/dec. have been reported for MOSFETs that simultaneously show a high on-state drive current [12]. An increase in the In content will enhance the electron mobility, but due to the narrower band gap, also minority carrier may start to affect the dynamic response [13]. Besides, the reduced band gap will strengthen the probability for tunneling, in particular, at the high-field drain-side, what may lead to increased leakage current. The III–V growth technology offers a solution to this limitation. Thin InAs channels may be used where the quantum confinement increases the effective band gap to reduce the possibility for tunneling [14]. The source/drain band structure may further be tailored using epitaxial heterostructures, like InGaAs/InP [15], or undoped spacer layers to suppress the tunneling contributions [16]. These approaches have demonstrated substantially improved performance with a reduced off-state leakage current [17].

2.2. RF-devices

III–V transistors have traditionally a very strong position in the area of RF-technology based on the high electron mobility and the low noise levels that can be achieved using epitaxial heterostructures. The introduction of a gate dielectric into the transistor architecture will allow for a better scalability of the gate length of the III–V FETs below 30 nm and reduce the gate leakage what is required for large scale integration. This development has also been initiated for the HEMT structures [18]. The development towards logic functionality, including p-type devices and the co-integration with the maturing n-type transistors on Si substrates, will provide further flexibility in RF-circuit design as well as reduced cost, what is essential to reach a larger market segments. It is hence natural to carefully consider the RF-options for III–V MOSFET technology.

The key metrics for RF-devices are defined differently as compared to logic devices. Nevertheless, they still connected to the transport properties within the channel and the electrostatic control provided by the transistor architecture. Much high-k technology development for logics is applicable also to RF-devices, but a few aspects will need further attention as discussed in the following sections. A high transconductance, g_m, is essential as it will determine the gain and influence the application frequency bandwidth. Further metrics include the intrinsic voltage gain, defined as the ratio between the transconductance and the output conductance, g_m/g_o, that is essential to increase the transistor high-frequency properties. A high breakdown voltage will increase the power capability of the transistor and a low on-resistance will reduce parasitic loss. The high-frequency metrics, f_t, f_{max}, finally describe the maximum frequencies where current and power gain, respectively, can be achieved balancing the gain and losses. With respect to the quality of the dielectric layer, transistor metrics like the g_m-frequency dispersion and the $1/f$-noise needs consideration and further optimization.

Clearly, the quality of the high-k gate dielectric and its interface to the semiconductor is essential to obtain excellent RF-performance of III–V MOSFETs also considering the here defined set of RF-metrics. In particular, we need to consider the electrical properties over a wider range of biases as compared to the logics, since the RF-transistors should operate at a higher drain bias. In Fig. 2, we show data for the leakage currents measured for Al_2O_3/HfO_2 bilayer gate dielectric deposited by Atomic Layer Deposition (ALD) at 300/100 °C that may serve as representative values for status in the field. In the data, we clearly identify an initial bias region with trapping followed by a bias region with increased leakage and defect creation before we finally reach destructive breakdown. It is at present, however, not clear to what