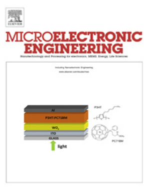
Microelectronic Engineering 147 (2015) 285–289

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee



# Integrated films of transition metal oxides for information technology

Alexander A. Demkov [a,*], Patrick Ponath [a], Kurt Fredrickson [a], Agham B. Posadas [a], Martin D. McDaniel [b], Thong Q. Ngo [b], John G. Ekerdt [b]

[a] *Department of Physics, The University of Texas at Austin, Austin, TX 78712, USA*
[b] *Department of Chemical Engineering, The University of Texas at Austin, Austin, TX 78712, USA*

ARTICLE INFO

*Article history:*
Received 18 March 2015
Received in revised form 12 April 2015
Accepted 13 April 2015
Available online 20 April 2015

*Keywords:*
Ferroelectrics
Monolithic integration
MBE
ALD
Density functional theory

ABSTRACT

The recently developed ability to grow layers of transition metal oxides with atomic precision by means of physical vapor deposition has opened up a possibility of monolithic integration of these oxides on semiconductors. Here we review the recent progress in integrating ferroelectric films with Si and Ge, and their potential applications in electronics and nanophotonics. Perovskite films described in the talk were grown by molecular beam epitaxy (MBE) and, when possible, chemical routes were tested *via* atomic layer deposition (ALD). Design of the structures and analysis of the experimental results were aided by density functional theory (DFT).

## 1. Introduction

Thin films of ferroelectric oxides grown directly on semiconductors have possible applications in non-volatile memory technology and nanophotonics. Nonvolatile semiconductor memories are essential in our daily lives, as large-capacity flash memories are used in solid state drives (SSD) of personal computers, mobile devices, digital cameras, moving-picture-experts-group (MPEG) audio players, universal-serial-bus (USB) memories, and other devices. Electrically erasable and programmable read-only memories (EEPROMs) and ferroelectric random access memories (FeRAMs) are used in wireless railway passes and IC (integrated circuit) or smart cards [1].

Among the new types of non-volatile memory, FeRAMs were the first to enter production. The most attractive feature of FeRAM is its low power consumption, which cannot be achieved by any other non-volatile memory. Because of this, FeRAMs have successfully competed even with flash memories, which require over 20 V for both write and erase operations. As FeRAM needs less than 2 V, the voltage-pump-up circuit can be eliminated. Also, writing speed and the maximum number of rewrites of FeRAMs are, respectively, at least two and six orders of magnitude greater than those of flash memory. The main problem of this type of ferroelectric memory is that it uses a separate ferroelectric capacitor in addition to a transistor (see Fig. 1(a)), and thus is difficult to scale to high density.

A pure transistor-type ferroelectric memory cell has a structure similar to that of a MOS transistor but with the gate oxide replaced with a ferroelectric oxide (see Fig. 1(b)). Such a device would be competitive with DRAM in terms of memory bit density. However, at present, the ferroelectric films used in transistor-type ferroelectric memories have a thickness of about 100 nm, which is too thick for gigabit-scale integration. Thus a thin ferroelectric film in monolithic integration with a conventional semiconductor is very attractive, particularly if long-term retention is not a critical issue such as in non-volatile caches for SSDs.

In addition, the large effective Pockels coefficient $r_{eff} = 148$ pm $V^{-1}$ (linear electro-optic effect) for high-quality epitaxial $BaTiO_3$ (BTO) films on Si distinguishes BTO as a highly promising material for integrated silicon nanophotonics [2,3]. Since the first successful integration of perovskite oxides on Si [4] and the successive demonstration of ferroelectric functionality [5], electro-optic activity [2], and devices [3], it has been found that these properties are strongly dependent on the crystalline structure of ferroelectric BTO. In order to achieve a strong electro-optic response, the film must have proper orientation with respect to the applied electric field [6], and be able to sustain a strong electric field without breakdown [7].

Monolithic integration of BTO on Si is enabled by molecular beam epitaxy (MBE) through the use of buffer layers, including BaO [8], $Ba_{0.7}Sr_{0.3}TiO_3$ [9], and most commonly, $SrTiO_3$ (STO)

---

[*] Corresponding author.
*E-mail address:* demkov@physics.utexas.edu (A.A. Demkov).

http://dx.doi.org/10.1016/j.mee.2015.04.090

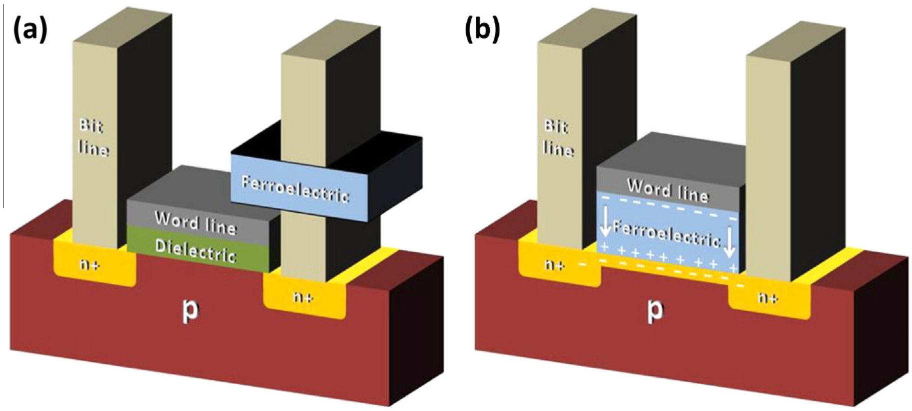


**Fig. 1.** (a) The structure of a 1T-1C FeRAM and (b) a transistor-type FeRAM. In (a) a ferroelectric material replaces the dielectric of the capacitor, while in (b) it replaces the dielectric of the transistor.

[2,5,10]. In what follows we shall describe our recent efforts to integrate ferroelectric BTO on Si and Ge using MBE and ALD.

## 2. BTO on Si by MBE

The epitaxial integration of $BaTiO_3$ (BTO) on Si(001) presents several challenges, particularly for applications requiring that the ferroelectric polarization be pointing out of plane. The lattice mismatch between BTO and Si is 4% (and even larger at typical growth temperatures) with the BTO compressed in-plane. While the direction of the mismatch is favorable for producing *c*-axis oriented BTO, the relatively large mismatch usually results in a very high defect density that can degrade the electrical properties of the film. Further, there has not yet been any successful direct growth of BTO on Si as no suitable wetting interlayer that will enable direct epitaxy has been discovered. Another challenge is the large thermal expansion mismatch between BTO and Si, with BTO having a thermal expansion coefficient about three times larger than Si. While BTO films have been grown on Si using various buffers [4,11–13], these typically produce *a*-axis oriented films as a result of the thermal expansion mismatch, which causes the BTO to experience tensile stress while cooling down through its Curie temperature. To resolve this problem, a combination of a suitable buffer that reduces both lattice and thermal expansion mismatch, and slow cool down to reduce stress is necessary to obtain *c*-axis oriented films on Si.

Our strategy is to use a fully relaxed layer of STO grown on Si as a pseudosubstrate for the subsequent BTO deposition. Though initial attempts to grow epitaxial STO directly on Si were only partially successful [6], McKee and co-workers have introduced a growth process that resulted in device quality STO films [14]. The key of this approach is to use 1/2 monolayer of Sr as a dual purpose template layer. First, the presence of Sr inhibits the oxidation of Si in a wide window of temperature and oxygen pressure. Second, the template results in wetting of Si by STO, enabling two dimensional growth [8]. The chemical mechanism of this effect is in the formation of an interfacial Zintl intermetallic that allows a low energy transition from the covalent bonding of Si to the ionic bonding of the oxide [15,16]. The lattice mismatch between BTO and relaxed STO still induces compressive strain that stabilizes out of plane orientation of the BTO film with a significantly reduced lattice mismatch of 2.2%, as well as a reduced thermal expansion mismatch such that BTO now experiences favorable compressive stress during cool down (the BTO thermal expansion coefficient is slightly smaller than the STO thermal expansion coefficient). To further reduce the lattice mismatch between BTO and STO, we can also anneal the STO pseudosubstrate in oxygen prior to BTO deposition to allow for plastic relaxation of the STO on Si as a result of $SiO_x$ interlayer formation. We have shown that STO films on Si annealed in this manner result in an in-plane lattice constant slightly larger than that of bulk STO [17]. By using this approach of tailoring the heterostructure layers and their interfaces, we show that we can overcome lattice and thermal expansion mismatch issues and grow *c*-axis oriented BTO films on Si with thicknesses up to 20 nm.

Lightly doped epi-grade Si(100) is cut into $20 \times 20\ mm^2$ pieces and degreased using a sequence of acetone, isopropanol and deionized water for 5 min each with sonication. After drying, the substrate is then exposed to ultraviolet/ozone for 15 min to remove organic contaminants before being loaded into the MBE growth chamber. The Si substrate is then outgassed at 675 °C for 10 min then dosed with 2 monolayers of Sr from an effusion cell followed by heating to 825 °C to desorb the native silicon oxide using the so-called Sr deoxidation process [18]. After achieving a clear $2 \times 1$ surface reconstruction characteristic of a clean Si(100) surface as observed in reflection-high-energy electron diffraction (RHEED), the sample is cooled to 575 °C and then dosed with additional Sr to form the Zintl phase template comprised of 1/2 monolayer Sr (surface has $SrSi_2$ stoichiometry) that is necessary for perovskite growth on Si(100). The characteristic RHEED pattern for the Zintl template layer is shown in Fig. 2(a). At moderate temperature, this Zintl phase template protects Si from oxidation and allows for nucleation and layer by layer growth of STO.

The Sr-templated Si substrate is cooled to 200 °C and then molecular oxygen is allowed to flow into the DCA 600 MBE chamber to a pressure of $8 \times 10^{-8}$ Torr. A three-unit cell STO seed layer is first deposited at 200 °C from Sr and Ti effusion cells calibrated to have the same flux ($\sim$1 monolayer per min). The film is barely crystalline at this growth temperature. The sample is then heated in vacuum to 575 °C, causing the seed layer to fully crystallize [17]. Additional STO is deposited until a total thickness of 6 nm is reached at which STO is already fully relaxed to its bulk lattice constant. After the STO growth, the substrate is heated at 20 °C/min to 700 °C while simultaneously ramping the $O_2$ pressure to $5 \times 10^{-6}$ Torr. When the target $O_2$ pressure and substrate temperature are reached, BTO growth by means of alternating monolayer dosing of Ba and Ti is initiated, with Ba first and Ti last. The entire growth process is monitored *in situ* by RHEED to ensure high crystallinity and stoichiometry. Fig. 2(b) shows a RHEED pattern after growth of a 20 nm BTO film on STO/Si. For films thicker than 5 nm, the growth was paused for 10 min after every 5 nm of growth. By doing these intermediate anneals, the high surface crystallinity is maintained throughout the entire growth process. After the desired thickness of BTO is grown, the sample is cooled at 5 °C/min in $O_2$ to room temperature. After growth, X-ray