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Deducing the apparent flat-band position V_{afb} and the doping level of large area single layer graphene MOS capacitors

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ABSTRACT

A capacitance–voltage (CV) study on large area CVD single layer graphene MOS capacitors has been carried out. The CV features are carefully examined to reveal the electronic origins of the observed frequency and bias dependence. In this study we investigate the frequency dispersion, propose the definition and extraction of the apparent flat-band V_{afb}, and finally perform the low temperature CV measurement to deduce the doping level of the graphene MOSCAPs.

1. Introduction

Novel two-dimensional materials have recently emerged as the main focus of advanced electronics device research. Despite well understood and documented transistor results, detailed CV studies on graphene MOS capacitors have been sparse and mostly theoretical due to difficulties of forming high quality oxides and robust MOS devices on large area graphene. In this work we demonstrate low temperature ALD oxide growth on large area CVD graphene and present in-depth CV characteristics of the graphene capacitors.

2. Experiment

Large area CVD mono-layer graphene was transferred onto silicon substrate with 300 nm oxide thickness as the starting wafer. Gate oxide films were deposited on top of graphene using low temperature atomic layer deposition (ALD) process optimized for physical adsorption [1]. The lack of chemically reactive sites on ideal graphene surface hinders the adsorption and nucleation of the ALD precursors in conventional growth conditions. In order to obtain closed dielectric layers with minimum thickness, it is necessary to shift the growth regime from chemisorption to physisorption by lowering the growth temperature. In our experiment, sample A received 15 nm ALD Al_2O_3 at 150 °C while sample B received 15 nm ALD Al_2O_3 at 150 °C and additional 10 nm ALD HfO_2 at 250 °C. To contact the CVD graphene, ohmic regions were defined by contact lithography followed by oxide removal. Ti/Pd was deposited as metal contacts to graphene and finally TiN was used as top metal gates. The structure of the graphene MOSCAP and its CV response are shown in Fig. 1. The multi-frequency CV traces are recorded with an HP 4284 LCR meter.

3. Electrical results and analysis

The first impression of the graphene MOSCAP CV (Fig. 1) is the small depletion dip, which can be attributed to the bandgap-less property and the density-of-state capacitance (quantum capacitance C_q) of graphene [2]. To get a good handle on the CV response and to estimate the graphene doping level, we will follow the analysis below.

3.1. Frequency dispersion and the apparent flat-band position

Multi-frequency CV plots of Fig. 2(a) of sample A and Fig. 2(b) of sample B show significant frequency dispersion across most of the voltage range, especially at bias points away from Dirac point. Such bias or field dependent dispersion in the accumulation regime typically indicates charge exchange with the oxide border traps [3–5].

Oxide border traps are defect states in the oxide or dielectrics that are close to the semiconductor interface and capable of

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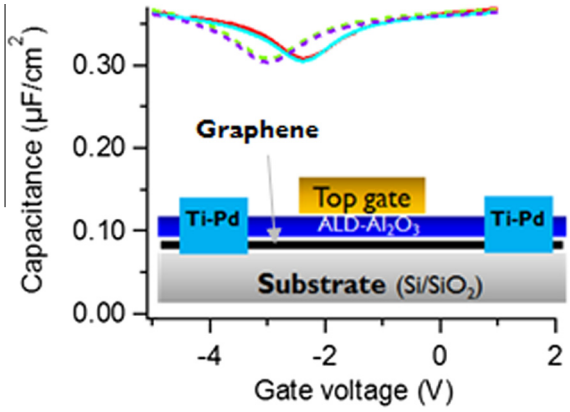

Fig. 1. Bi-directional CV traces and the MOSCAP cross-section structure.

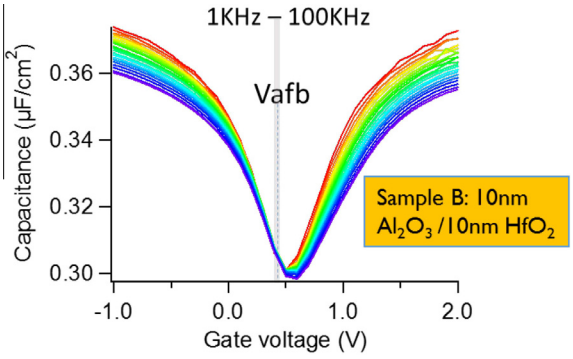

Fig. 2b. Multi-frequency CV traces of sample B. The minimum frequency dispersion window and the flat-band voltage are to the left of Dirac point. The underlying graphene therefore exhibits p-type doping.

exchanging carriers with the conductive materials nearby. The time constants of the border traps can vary by several orders of magnitude, from micro-seconds to hundreds or thousands of seconds [6]. Typical CV measurements use small ac signals from 100 Hz to 1 MHz and cover mainly the time constants of near-interface traps. For conventional MOS devices the increase in frequency dispersion with gate bias in accumulation region can be explained by the convolution of sharper band bending and the defect bands in the oxide [7]. In the case of a metal-oxide–graphene CV, which appears to be ambipolar, there exists a narrow bias window by which the amount of frequency dispersion is at its minimum, as can be seen in Figs. 2(a) and 2(b). We believe that the observed dispersion minima suggest the presence of minimal electric field across the oxide at the corresponding gate biases and propose the apparent flat band voltage (V_{afb}) concept as illustrated by Fig. 2(c). To better grasp the connection between frequency dispersion and oxide E-field one could start by assuming the M-O–graphene system is initially at the apparent flat-band condition. The basic electrostatics of MOS dictates that if additional negative gate bias is applied at the gate, the trapping of holes in the oxide prevails over that of electrons, and vice versa when additional positive bias is applied, as indicated in Fig. 2(c). Due to its bandgap-less feature, a graphene sheet supplies both types of carriers when biased at few kTs (~80 meV at room T) above or below Dirac point, and a continuous transition from electron trapping to hole trapping is foreseen. Now we will take a look at dispersion. It has been proposed that CV frequency dispersion is linked to oxide trapping governed by the mechanism

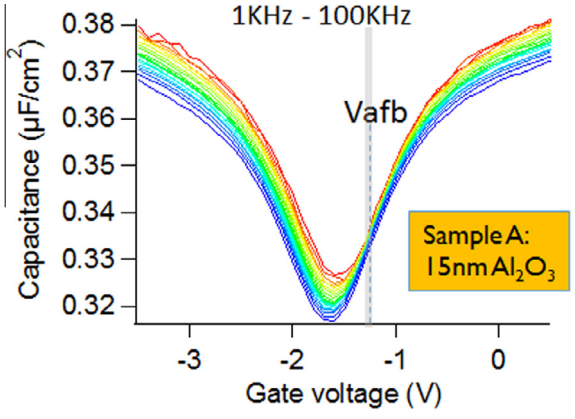

Fig. 2a. Multi-frequency CV traces of sample A. A narrow window of frequency dispersion minimum indicates the apparent flat-band voltage. The underlying graphene exhibits n-type doping.

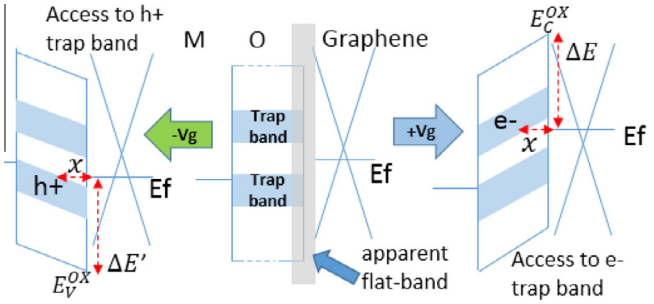

Fig. 2c. The apparent flat-band position V_{afb} by which minimum E-field is established across the graphene-oxide interface. Bending the oxide band by applying bias would induce electron or hole trapping at the defect/trap band and render frequency dispersion. Notice in definition the apparent flat-band is not the same as the conventional flat-band, which is based upon three dimensional semiconductors with carrier distribution along the gated E-field direction.

of carrier tunneling [5]. The trapping time constant τ is inversely proportional to the carrier density N_S at the interface and exponentially dependent on the trap location x and the square-root of the energy gap ΔE between the graphene Fermi-level and the oxide band edge:

$$\tau(x) = \frac{\exp\left(\frac{2x\sqrt{2m^*\Delta E}}{\hbar}\right)}{N_S V_T \sigma} \quad (1)$$

V_T, σ and m^* are the carrier thermal velocity, oxide trap capture cross section and the effective electron mass in the oxide, respectively. When a positive bias is applied in addition to the flat-band voltage, the electron density N_S increases while the energy gap between the oxide conduction band edge and the graphene Fermi-level ($\Delta E = E_C^{OX} - E_f$) narrows, allowing for deeper tunneling of electrons (in x) under a given ac frequency ($f = 1/2\pi\tau$), as described by Eq. (1). Conversely, when the bias is pushed below V_{afb}, the gap between the oxide valence band edge and the graphene Fermi-level ($\Delta E' = E_f - E_V^{OX}$) decreases and the hole density increases, enhancing the tunneling of holes. Together with the existence of oxide defect/trap bands, as illustrated in Fig. 2(c), it is clear that sharper band bending would give carriers access to more traps at distances closer to the interface. This illustrates that moving away from the apparent flat band point in either direction would increase the probability of oxide trapping and the magnitude of frequency dispersion.

Since frequency dispersion can be viewed as changes in capacitance at a fixed bias or shifts in bias at a fixed capacitance, it can be argued that repeated dc sweeps would induce parallel shifts and