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Effective work function modulation by *sacrificial* gate aluminum diffusion on HfON-based 14 nm NMOS devices

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ABSTRACT

Sacrificial gate first process efficiency to further increase effective work function (WF_{eff}) towards P+ by metallic aluminum diffusion is demonstrated in this work by combining capacitance vs voltage (CV) measurements on beveled oxides with different spectroscopic techniques. Aluminum diffusion role on WF_{eff} is evidenced and is found to be simultaneously dependent of as-deposited aluminum dose and annealing temperature.

1. Introduction

The scaling of MOS transistors while keeping overall performances led to the inclusion of high-κ metal gate (HKMG) stack in the conventional SiO_2/Poly-Si gate stack. The effective work function (WF_{eff}) values of metal electrodes must satisfy the V_{TH} requirements of specific devices. In undoped-channel 14 nm Fully-Depleted Silicon on Insulator (FD-SOI) devices, WF_{eff} at only ≈100 mV from the midgap are required [1,2]. In order to reach the ΔWF_{eff} specification for PMOS, deposition of Al_2O_3 as high-κ dielectric, or above the high-κ layer [3] and insertion of metallic aluminum in TiN gate [4] have already been proposed to shift the WF_{eff} towards P+. Nevertheless, opposite shift of the Al-based metal workfunction towards N+ limits the benefit of dipoles induced by Al diffusion to the high-κ/SiO_2 interface. Even though aluminum ion implantation is very effective in achieving PMOS low V_{TH}, it can induce gate leakage degradation by Al diffusion too deeply near SiO_2/channel interface [5]. In this work, we evaluate the impact of Al on WF_{eff} and Equivalent Oxide Thickness (EOT) in a *sacrificial metal gate-first approach*. Moreover, the Al diffusion is studied by X-ray Photoelectron Spectroscopy (XPS) and X-ray Fluorescence (XRF) measurements as a function of the aluminum dose, the composition of the TiN layers and the annealing temperature.

2. Device fabrication

Silicon trench isolation (STI) and P-Well implants were carried out on Si (100) wafers before HKMG stack deposition. The gate dielectrics consist of interlayer dielectric followed by a 2 nm thick HfO_2 layer deposited by Atomic Layer Deposition, and decoupled plasma nitridation. Interlayer dielectric is either 1 nm thick SiON for nominal devices or a beveled thermally grown SiO_2 (Fig. 1) to get rid of Si/SiO_2 interface fixed charges ($Q_{SiO_2/Si}$) in WF_{eff} extraction. Then, the sacrificial Si/TiN/Al/TiN gate stacks (Si on top) with different Al doses (0 Å, 2 Å, 6 Å) and TiN compositions ($[N_2]/([N_2]+[Ar])$ = 0.5, 0.7 and 1) were deposited, followed by a thermal treatment under N_2 atmosphere at 900 °C or 1000 °C in order to activate the diffusion of Al into the HfON/SiON stack. The sacrificial gate stack is then removed by wet etching. Finally, a Poly-Si/TiN electrode is deposited, followed by gate patterning, as illustrated in Fig 2. All metal layers were deposited in Radio Frequency Physical Vapor Deposition chambers. Samples description is summarized in Table 1. Devices were completed with S/D formation, S/D dopant activation annealing at 1005 °C, NiPt silicide and a 400 °C forming gas annealing.

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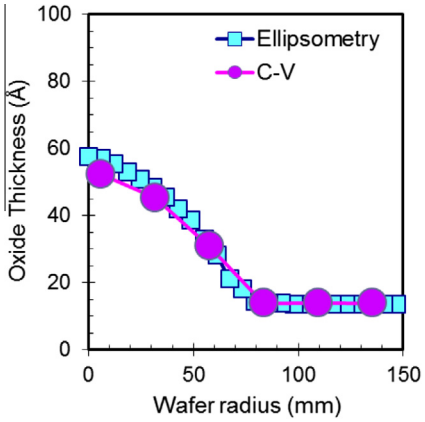

Fig. 1. Ellipsometry and CV measurements on bevel oxide along a 300 mm wafer.

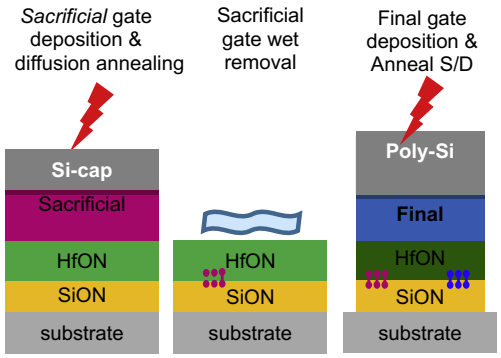

Fig. 2. Sacrificial gate first approach scheme.

Table 1
Description of devices with aluminum in sacrificial gate.

	IL oxide	TiN composition $N_2/(Ar + N_2)$	Al dose (Å)	Diffusion annealing
No sacrificial	Bevel	–	–	Only S/D annealing
TiN80-w/o Al	Bevel	0.5 (51.3 N-at%)	0	900 °C
TiN/Al2.0/TiN	Bevel	0.5 (51.3 N-at%)	2.0	1000 °C
TiN/Al2.0/TiN	Nominal	0.5 (51.3 N-at%)	2.0	900 °C
TiN/Al6.0/TiN	Nominal	0.5 (51.3 N-at%)	6.0	900 °C
PS/Al2.0/PS	Nominal	0.7 (52.6 N-at%)	2.0	900 °C
PS/Al6.0/PS	Nominal	0.7 (52.6 N-at%)	6.0	900 °C
FN/Al2.0/FN	Nominal	1 (54.6 N-at%)	2.0	900 °C
FN/Al6.0/FN	Nominal	1 (54.6 N-at%)	6.0	900 °C

3. Electrical characterization

EOT and V_{fb} were extracted by fitting Poisson Schrödinger quantum simulations with experimental CV measurements on different dies along the wafer [6]. Assuming (1) no bulk charge in the dielectrics and (2) independence of V_{fb} with HK thickness, V_{fb} dependence with EOT is given by Eq. (1), where ε_{ox} is the dielectric permittivity of SiO_2, WF_m and WF_{Si} are the metal and silicon work function relative to vacuum, respectively, and δ denotes the sum of interfacial dipoles [7]. WF_{eff} expression is then calculated from V_{fb} using Eq. (2):

$$qV_{fb} = WF_m + \delta - Q_{SiO_2/Si}\frac{EOT}{\varepsilon_{ox}} - WF_{Si} \quad (1)$$

$$WF_{eff} = qV_{fb} + WF_{Si} \quad (2)$$

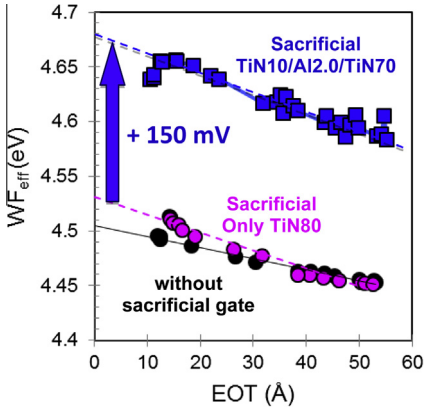

Fig. 3. WF_{eff} vs EOT for devices with beveled oxide: with Al (annealed at 1000 °C) and without Al (annealed at 900 °C) in sacrificial gate and w/o sacrificial gate. TiN and Al thicknesses are in Å.

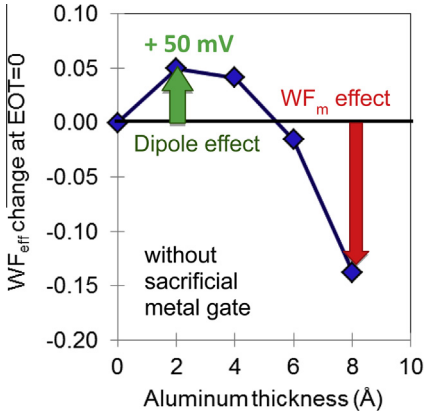

Fig. 4. Impact of Al thickness inserted in final gate electrode.

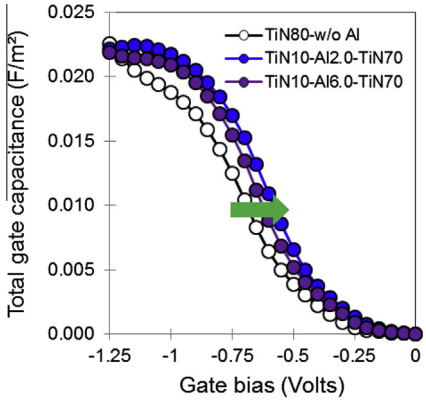

Fig. 5. CV curve as a function of Al thickness in sacrificial gate approach (diffusion annealing at 900 °C). TiN and Al thicknesses are in Å.

The plot WF_{eff} vs EOT for devices with beveled oxide is shown in Fig. 3.

The extrapolation of WF_{eff} to zero EOT allows the assessment of only WF_m and δ, without the impact of Si/SiO_2 interface fixed charges [8]. Compared to devices for which Al was not included in sacrificial gate stack, we note that Al in *sacrificial gate* shifts the WF_{eff} ≈150 meV towards P+. Compared to the *final metal approach* (Fig. 4), (i.e., metallic aluminum deposited in the Poly-Si/TiN final electrode and no sacrificial gate), the WF_{eff} shift