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Electrical characteristics of ALD La_2O_3 capping layers using different lanthanum precursors in MOS devices with ALD HfO_2, $HfSiO_x$, and HfSiON gate dielectrics

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ABSTRACT

We have investigated the electrical characteristics – flat band voltage (V_{FB}) shift, equivalent oxide thickness (EOT) scaling and charge trapping – of atomic layer deposition (ALD) La_2O_3 capped high-*k* gate dielectrics (HfO_2, $HfSiO_x$, and HfSiON) in the metal-oxide-semiconductor (MOS) device structure, where two different lanthanum precursors – ① lanthanum formamidinate, $La(fAMD)_3$, and ② lanthanum beta-diketonate, $La(thd)_3$, – were used for ALD capping layer. Regardless of precursors, La_2O_3 capping layer on the ALD high-*k* films leads to negative V_{FB} shift and thinner EOT as increasing capping thickness. However, more shift and further EOT scaling are observed with La_2O_3 thin film using $La(fAMD)_3$. In addition, La_2O_3 capping layer using $La(fAMD)_3$ precursor shows lower interface state density (D_{it}) and stronger immunity against charge trapping than La_2O_3 capping layer with $La(thd)_3$ precursor. Similar trends are attained with Si containing HfO_2 – $HfSiO_x$ and HfSiON, but amount of V_{FB} shift and EOT reduction is smaller than that of HfO_2-based device, resulting from suppressed La-diffusion due to stronger Si–O bonds as well as nitrogen blocking in the dielectrics.

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1. Introduction

A successful adoption of high-*k*/metal gate (HKMG) technology into manufacturing logic devices with gate last process has driven further implementation into other applications such as dynamic random access memory (DRAM) [1]. Even though device requirement of peripheral transistors in DRAM is not as tight as in the logic transistor case, alternative material and process integration should be still considered to achieve low and symmetric threshold voltage (V_{TH}) for advanced DRAMs because the peripheral transistor process is completed in advance, and subsequent capacitor fabrication steps including high thermal process could significantly degrade the properties of HKMG in peripheral transistors. Therefore, gate-first (GF) process is still cost-effective for DRAMs if solutions to suppress V_{TH} roll-off, reduce leakage current and scale EOT are provided. Material-oriented solution using group IIA elements in the periodic table such as La can induce negative V_{FB} shift (i.e., lower V_{TH}) for GF-nMOS device because diffused La elements through high-*k* gate dielectric cause dipole formation at the Si substrate and interfacial layer [2–5].

Several ALD precursors such as $La(N(SiMe_3)_2)_3$, $La(iPRADL)_3$, and $La(iPrCp)_3$ to deposit La_2O_3 capping layer on the high-*k* gate dielectrics have been demonstrated with negative V_{FB} shift and scaled EOT [6–9]. Electrical properties of n-channel MOS devices are substantially affected by ALD La precursor, gate dielectrics and process integration. Even though several studies on ALD La_2O_3 capping layer have been reported, there are few reports on the systematic investigation on the effects of dielectrics, process temperature, and precursor on EOT and V_{FB} in MOS devices.

We investigated the impact of ALD precursors on V_{FB} shift, EOT scaling and charge trapping in the ALD La_2O_3-capped HKMG device structures. Our result suggests that besides process optimization, the precursor is also important to attain improved electrical properties of GF-based nMOS device applications.

2. Experiment

After device isolation, interfacial layer (IL) was grown during the pre-gate clean step. HfO_2, $HfSiO_x$, and HfSiON gate dielectrics were deposited by ALD using precursors (TEMAHf for Hf, TEMASi for Si), oxidant (H_2O, O_3), purging gas (Ar) and nitrogen source (NH_3) for nitridation at a temperature in the range about 300 °C to 350 °C. ALD La_2O_3 capping layer was prepared by $La(fAMD)_3$ and $La(thd)_3$ precursors. Some samples received sputtered La_2O_3

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layer for comparison, where La was deposited first, followed by air exposure. Next, TiN gate electrode was DC-sputtered, followed by gate patterning and post metal annealing at various conditions. Final forming gas anneal (FGA) was carried out at 400°C for 15 min [10]. The electrical properties were characterized by capacitance voltage (*C–V*) measurement at a frequency of 100 kHz before and after FGA using an Agilent E4980A CV-meter and a HP 4145B parameter analyzer. D_{it} values were attained using the conductance method.

3. Result and discussion

Considering growth rate behaviors as a function of various deposition temperatures, ALD La_2O_3 deposition temperatures using $La(fAMD)_3$ and $La(thd)_3$ were chosen at 150 °C and 275 °C, respectively, as shown in Fig. 1. The *C–V* characteristics of MOS devices with 1 nm thick-ALD La_2O_3-capped HfO_2 gate dielectrics are shown in Fig. 2. Compared to non-capping device, negative V_{FB} shift and higher gate capacitance are observed at the devices with La_2O_3capping. Between two precursors, $La(fAMD)_3$-based device shows more negative V_{FB} shift as well as higher capacitance. Fig. 3 compares V_{FB} shifts on HfO_2 as a function of ALD La_2O_3 thickness. Regardless of precursors, increasing La_2O_3 thickness induces more negative V_{FB} shift, but the shift using La_2O_3 prepared by $La(fAMD)_3$ is more substantial. The correlation between EOT and V_{FB} shift is presented in Fig. 4. Compared with non-La_2O_3 capping, ALD La_2O_3 capping induces negative V_{FB} shift as well as EOT scaling. However, compared to $La(thd)_3$ precursor, further V_{FB} shift (>50 mV) and EOT scaling (~0.1 nm) are attained with $La(fAMD)_3$ precursor. These results are attributed to lower deposition temperature and different optimal oxidant pulse time. Fig. 5 shows V_{FB} shifts as a function of various post annealing temperatures. It indicates that La diffusion becomes saturated over 700 °C irrespective of precursors, guiding a maximum process temperature through the whole process integration. La needs to be diffused into IL for the dipole formation, leading to V_{FB} shift. This saturation of the V_{FB} shifts with respect to process temperature suggests that the process temperature of the device integration containing La_2O_3 capping layer can be lowered down to 700 °C. Regardless of precursors, increasing La_2O_3 capping layer causes slight increase

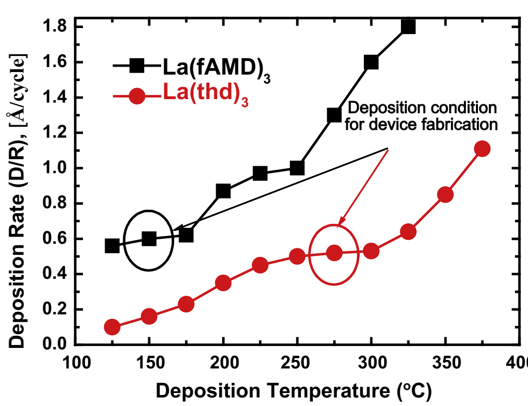

Fig. 1. ALD deposition rate of La_2O_3 films using different precursors as a function of process temperature.

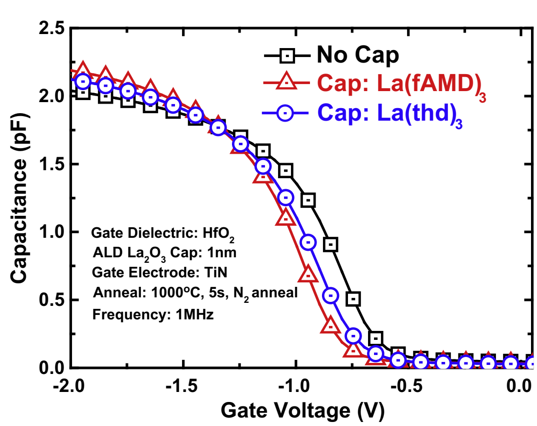

Fig. 2. C–V characteristics of MOS devices with La_2O_3-capped HfO_2.

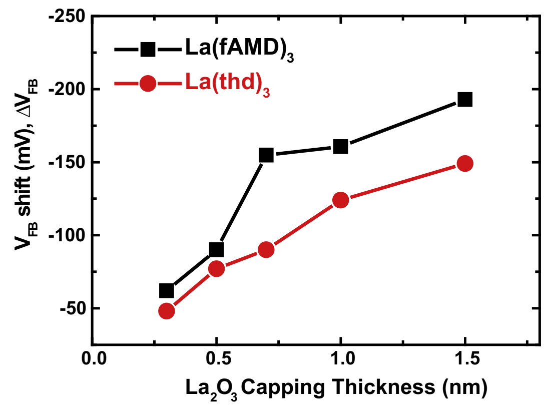

Fig. 3. V_{FB} shift with increasing La_2O_3 capping layer on the HfO_2 gate dielectric.

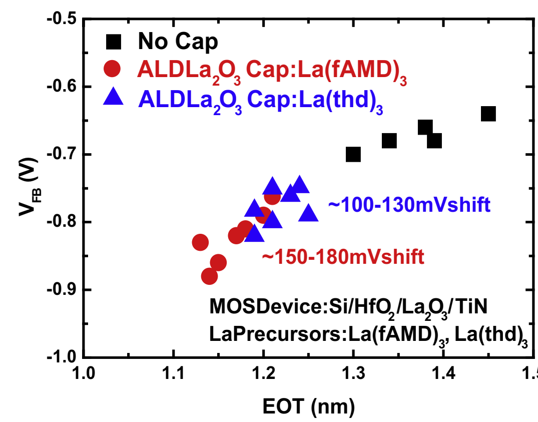

Fig. 4. The effects of La_2O_3 capping and ALD La precursors on EOT vs V_{FB} behaviors.

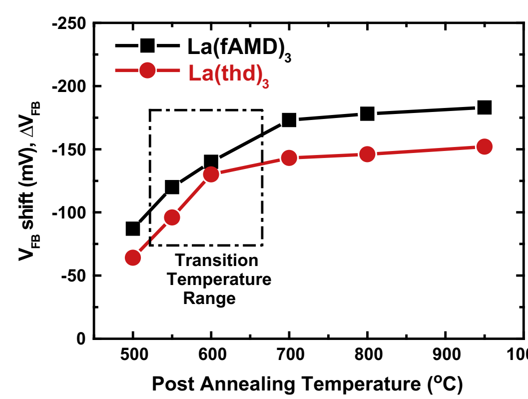

Fig. 5. V_{FB} shift as a function of post annealing temperatures on MOS capacitor with La_2O_3–capped HfO_2 gate dielectric.