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Inductively coupled plasma etching of tapered via in silicon for MEMS integration

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ABSTRACT

An ICP plasma etching technique for fabrication of tapered vias on silicon substrates has been developed by means of single patterning and etching process. Experimentally, effects of parameters including ICP power, chamber pressure, gas ratio and RF bias power were investigated for their impact on etch rate, selectivity, profile and surface roughness. Monotonic profile angles in the range of 60–80° have been achieved on 10–50 μm wide vias through adjustment of the C_4F_8/SF_6 ratio and optimization on other key parameters. We found that addition of O_2 controlled lateral etch rate only weakly, except when running the process at cryogenic temperature. Adjustment of the process powers was a significant factor in controlling sidewall roughness.

1. Introduction

There is a demand for increasing levels of integration and function density to meet the requirements of consumer applications, such as CMOS and MEMS components for high memory, high processing speeds and advanced functions in smart phones and other portable equipment. Compared to traditional wire-bonding methods, through-silicon vias (TSVs) provide a short interconnect path with a high density [1,2]. Therefore, in recent years conductive TSVs have become an important emerging technology for electrical connection of stacked devices in semiconductor industry as alternative to conventional wire bonding [1] and to connect and control stacked MEMS or combined MEMS-CMOS modules in order to save space (see Fig. 1).

For increased throughput and simplified etch requirements, silicon wafers can be thinned to 50–100 μm thick with a handle wafer for high density TSV applications. This reduces the aspect ratio (AR) required to etch TSVs and subsequent thin film depositing steps. Typical sizes of TSVs are in the range 5–50 μm in diameter and 50–500 μm depth. State-of-the-art wafer-level bonding techniques are able to integrate heterogeneous materials (e.g. III–V compounds, ferroelectric, etc) on a silicon base chip with multiple functions [2]. These pioneering ideas are also opening new research frontier for MEMS and optoelectronic integration. A controllable wide-angle range TSV (60–85°) technique with a wide material compatibility in order to facilitate void-free filling the via with contact metal is a preferred approach in this scenario.

The Bosch deep silicon etch (DSiE) process [3] is usually used to etch TSVs. This uses a high density plasma with cycling deposition and etch steps to provide a vertical profile (typical 88–90°) capable of high aspect ratios (AR) at high rate. The achievable angular range, however, is too limited to address tapered profile requirements. Through an isotropic etch, a tapered profile (<85°) can be achieved [4] but typically with an overhang at top of via – see Fig. 2. This overhang would result in void formation in subsequent seeding and filling steps. To realize a void-free via, this overhang may be removed by means of a subsequent maskless etch step [4,5], but it results in the loss of a few microns silicon on the surface and enlarges the critical dimension (CD) of the TSV [5]. Moreover the process may not be tolerated by unprotected device areas on the surface. Recently, it has been shown that a SF_6-O_2 chemistry may be used to realize an 80° via profile, but a 70° profile has proven difficult to achieve [6,7]. An anisotropic wet etch that is selective to the <1 1 1> planes, such as KOH, EDP or TMAH, may achieve a tapered profile but at a fixed angle 54.74° for <1 0 0> silicon wafers [8]. It is also limited to low AR, requires additional alignment to the crystalline plane and has restrictions on geometry (circular features being particularly challenging and often requiring corner compensation).

The focus of the work reported here was to develop techniques to achieve selectable tapered profile on an etched TSV profile by means of ICP etching. As a result, monotonic profiles in the range

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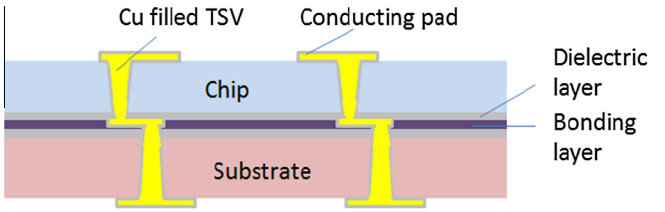

Fig. 1. Illustration of MEMS 3D integration and wafer-level packaging with a typical TSV technology.

of 60–80° for subsequent void-free filling have been successfully achieved on 10–50 μm wide vias.

2. Experimental

Etch experiments were carried out in an ICP etch system (Oxford Instruments PlasmaPro 100 Estrelas) as schematic of which is shown in Fig. 3 using a SF_6-C_4F_8 "mixed gas" chemistry. 4.5 μm thick photoresist (PR) masks were patterned on standard <100> silicon wafers using conventional photolithography. PECVD silicon oxide (SiO_2) was deposited on additional silicon wafers at 300 °C in order to check the etch selectivity to SiO_2.

ICP chamber pressures from 25 to 120 mTorr and total flows in the range of 100–1000 sccm were selected. The ICP source frequency was 2 MHz, and its power was set in the range of

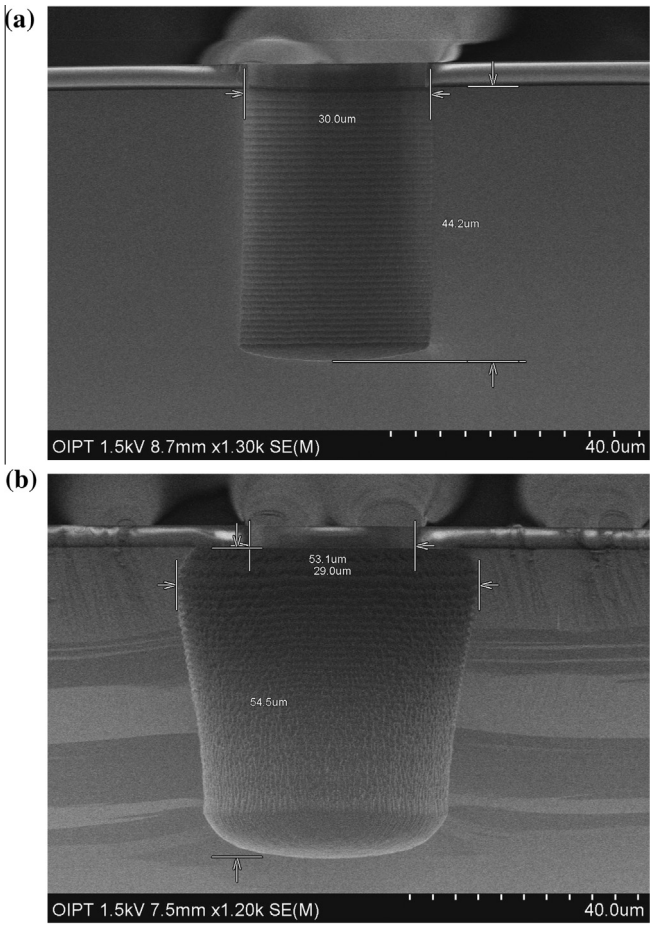

Fig. 2. Tapered via fabrication by two-step etching (a) after high-rate Bosch etch (18 μm/min); (b) subsequent SF_6/O_2 isotropic etch, 80° profile at a 30 μm via, but overhang at top.

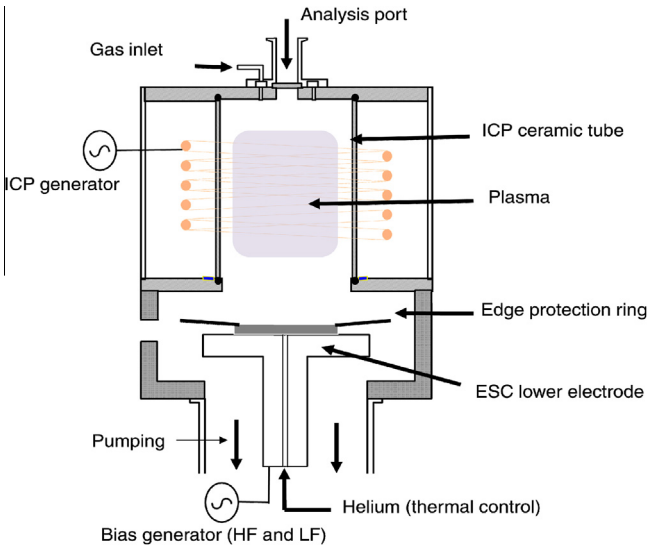

Fig. 3. Schematic of an ICP etch system.

1000–5000 W in order to generate a high density of fluorine (F) radicals in the plasma. RF bias powers in the range of 10 to 200 W were applied from either 13.56 MHz high frequency (HF) or 350 kHz low frequency (LF) generators to the lower electrode with an electrostatic chuck (ESC) to generate a self-biasing voltage to vertically attract ions from the plasma to the wafer surface. The DC bias voltage values mentioned in this paper were those supplied by the analog meters and software of the tools used [9]. The wafers were chucked on the lower electrode set at a temperature of 0 °C and controlled to within ±1 °C.

After etching, etch rate, selectivity, profile and surface morphology were investigated by means of a field-emission scanning electron microscopy (SEM) in order to develop the tapered via etch processes.

3. Results and discussion

In this paper, we described the development and characterization of plasma etching processes with various process conditions. A study was performed to analyze the effect of these key factors on the results.

3.1. Effect of chamber pressure and gas flow

Both etch rate and selectivity are calculated and plotted in Fig. 4(a) and (b). Higher pressure with a high SF_6 gas flow gave a faster rate and a higher selectivity because it supplied higher F radical concentrations which enhanced the chemical reaction with Si. As a result, an etch rate in excess of 10 μm/min was obtained on a 63° profile TSV etch, with sidewall roughness of <1 μm, as shown in Fig. 4(c). However, it was challenging to achieve steeper sidewall profiles due to a high lateral etch rate.

3.2. Effect of ICP source power

Fig. 5(a) and (b) indicate that raising ICP power also dramatically increases etch rate in the vertical direction but simultaneously decreases selectivity to mask materials. This decrease of selectivity could limit attaining the desired via etch depth. This is attributed to high ICP source power enhancing the dissociation and ionization of both SF_6 and C_4F_8. The increase of radicals and ions from SF_6 was higher than that from the polymer (C_4F_8)