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Thermo-mechanical characterization of copper through-silicon vias (Cu-TSVs) using micro-Raman spectroscopy and atomic force microscopy

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ABSTRACT

Thermo-mechanical reliability of through-silicon via (TSV) structures is affected by the residual stress, which is generated during thermal cycling in back end of line (BEOL) stack manufacturing, and by the 3D bonding processes. In this study, micro-Raman spectroscopy is employed for characterization of the local residual surface layer stress in Si due to the proximity of copper vias. We found that stress reduction in silicon in the vicinity of the TSVs is due to the relaxation after post-annealing. The residual thermal stress is relaxed more in the direction where the neighboring TSVs exist. Re-crystallization due to grain growth and also plastic and viscous behavior after annealing at high temperature might lead to higher stress relaxation that can impact on decreasing the keep-out zone (KOZ) size. Furthermore, the effect of post-annealing of Cu-TSVs in the generation of via protrusion is investigated. Cu protrusion mainly occurs due to the plastic and viscous behavior of Cu in the TSV. It was predicted from earlier publications, that the protrusion height is increasing with increasing the annealing temperature. However, we show that it might decrease at higher annealing temperatures of about 380 °C. This result can be associated with large modification of the copper grain growth and/or stress-induced grain sliding.

1. Introduction

In three-dimensional (3D) vertically stacked logic blocks, short vertical highly conductive interconnects (through-silicon vias) [1] replaced long wire bonding connections used in 2D integration [15,4,16]. Despite potential benefits of the through-silicon vias (TSVs) in 3D packaging and integrated devices, their fabrication processes and integration face several electrical and mechanical reliability challenges. Some of reliability issues are the result of residual thermal stress generated during manufacturing, testing [3], integration process steps, and operation of the TSV structures [4,5,1,16]. These reliability concerns are the consequence of coefficient of thermal expansion (CTE) mismatch between the TSV filling material, surrounding dielectric, and Si substrate [11]. Among the filling materials, copper is widely used due to its low resistivity and compatibility with back-end of line (BEOL) processing and interconnects [3,14]. However, the CTE of copper (~17.3 ppm/°C) is approximately six times greater than the CTE of silicon (~2.6 ppm/°C) at 20 °C [15,16,20]. This thermal mismatch translates into thermal strain/stress in the vicinity of respective interfaces around the TSV [15,8,13,16,17]. The stress level, in the TSVs and close to active electronic devices/components, is important since it can degrade the electrical performance of stress-sensitive devices adjacent to the TSVs [5]. It can drive crack growth, TSV protrusion [3], delamination at the interfaces of Si/SiO_2 [15,18] in 3D interconnects [6,12,13].

Therefore, for successful implementation of 3D integration [8], characterization of thermal stresses in and near the TSV structures, and also the prediction of potential electrical and mechanical reliability issues are essential [5]. This study focuses on: (1) the protrusion of Cu investigated by AFM, and (2) the thermal residual stress in Si investigated by micro-Raman spectroscopy.

In the present study, the effect of thermal annealing on protrusion of Cu was investigated with an AFM Dimension Extended D3000 exploited in tapping (AC) mode. In addition, Raman measurements were carried out with a commercial micro-Raman

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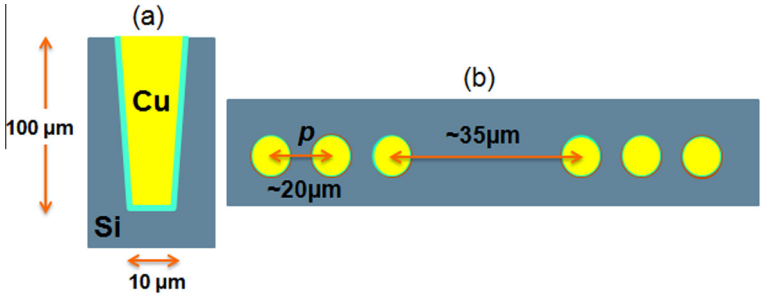

Fig. 1. The schematic view of copper vias geometry fabricated in (1 1 0) Si wafer plane. (a) Schematic of the cross section Cu-TSVs layout with 10 μm diameter and 100 μm depth. (b) Top-surface view of periodic layout of three copper vias with the pitch of 20 μm between the adjacent vias in the same group and ~35 μm between the neighboring vias of different groups respectively (*p*: pitch size between the neighboring vias).

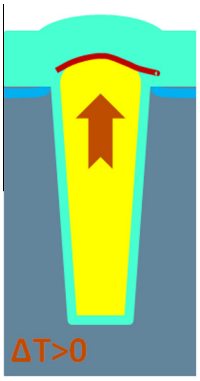

Fig. 2. Schematic illustration of the TSV protrusion under a positive thermal loading.

spectrometer (LabRam HR800 from HORIBA Scientific with 40× NUV Olympus BX-40) equipped with a 325 nm (HeCd) laser in back scattering configuration.

2. Results and discussions

2.1. AFM measurements on the extruded Cu via

The specimens investigated in this study contain periodic groups of three blind Cu vias (open only on one side) with 10 μm in diameter and 100 μm in depth, fabricated in (1 1 0) Si wafer plane (Fig. 1(a)) by Bosch process. Detailed description of the process was adapted from [23]. The distance between the adjacent vias (pitch) in the same group of TSVs is 20 μm and the pitch between different groups is approximately 35 μm as shown in Fig. 1(b).

Thermally-induced TSV height increase is known as "copper protrusion", "copper extrusion", "copper pumping" or "popup" [12,16]. The pumping phenomenon occurs when copper is forced out of the via as the consequence of high stress in the annealed copper [11] (Fig. 2). The magnitude of mechanical stress as a result of CTE mismatch depends on the material properties, which are determined by the material microstructure, such as the grain size and the crystal orientation [13]. Annealing either at room temperature (room temperature aging) or elevated temperature leads to grain growth due to grain boundary motion, which results in copper protrusion [21]. However, higher annealing temperatures were shown to lead to a more significant increase in the grain size [21]. It also develops plasticity or possibly visco-plasticity in the Cu vias [11], which can lead to a significant TSV protrusion [3], shown in Fig. 2.

For comparison of copper protrusion, 3D AFM topographical images of reference sample (before post-annealing) and post-annealed Cu-TSVs for 1 h at 250 °C, 300 °C and 380 °C with similar geometries are shown in Fig. 3 as an example. Following the annealing, the TSV surface became slightly domed and raised above the Si wafer surface. The permanent irreversible plastic

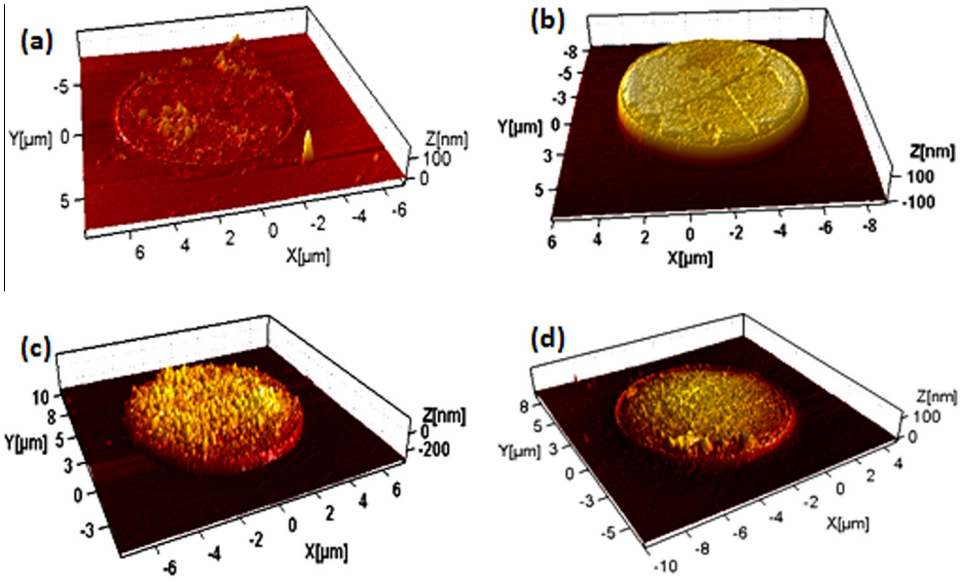

Fig. 3. Three-dimensional AFM topography of Cu-TSV (a) before post-annealing (reference), and post-annealed for 1 h (b) at 250 °C, (c) at 300 °C, (d) at 380 °C, respectively.