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Review Article

Fabrication of gated nano electron source for vacuum nanoelectronics

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ABSTRACT

Many kinds of attractive new applications, such as image sensors, stationary X-ray sources, and the column-less SEM, are investigated as post field emission displays that use a gated nano electron source. The fabrication of the gated nano electron source is overviewed from the conventional method to the latest one, especially in regarding to the gate formation process. Multi-stacked gate electrode formation using an etch-back method was developed recently, which is a very attractive method for generating a focused electron beam. The traditional Spindt-type emitter fabrication method is also being improved to the one that is easier and applicable to large area substrates. Using a double-layered photoresist as a lift-off layer and using HiPIMS sputtering instead of an e-beam evaporator was proposed. Thin film-type FEA fabrication is also improved to make vertically standing thin film by ion irradiation, which is applicable for making an emitter array on a large sized substrate.

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1. Introduction

The gated nano electron source (field emitter arrays: FEA) has been intensively investigated since the 1990s for application to the field emission display (FED). The Futaba Corporation started mass production of the 1st generation monochromatic FED [1] from the 90s and the 2nd generation full color FED [2] from 2006 by using a Spindt-type FEA. The mass production of larger display panels was also projected; one was a display that uses a nano-Spindt emitter made by Field Emission Technologies Inc. [3], and the other was one that uses a surface-conduction electron-emitter (SCE) made by SED Inc. [4]. However, companies gave up the commercialization after 2008. Although FED development declined, the gated nano electron source has been improved continuously and is still an attractive device for new applications, such as an FEA X-ray image sensor using CdTe that can detect not only the X-ray intensity but also the incident X-ray photon energy [5], a medical image sensor using a highly sensitive imaging device that has an FEA and a high avalanche rushing amorphous photoconductor (HARP) [6], a stationary X-ray source array for a medical tomographic system [7,8], a column-less scanning electron microscope (SEM) using a quintuple-gated FEA [9], and a field-emission based THz wave generator [10]. These applications are possible thanks to a breakthrough in the fabrication of the gated FEA. The technologies developed before 2001 are well described in Refs. [11,12]. In this paper, recent innovative nano-fabrication of the gated FEA, especially of the vertical-type FEA, which includes Si and Spindt-FEA, will be overviewed with a historical explanation of FEA fabrication.

2. Silicon emitter fabrication

Crystalline silicon was widely used for making vacuum micro- and nano-electronics device because of its well-developed fabrication process used in semiconductor device fabrication. In an early stage, a single crystalline silicon wafer is wet etched to form field emitter arrays [13]. Isotropic etching and orientation-dependent etching is extensively developed. It was, however, very difficult to achieve good uniformity in a large area substrate when using wet etching. After the dry etching process was applied, silicon emitter fabrication development accelerated.

2.1. Formation of single crystalline silicon emitter using dry etching

Betsui [14] developed a method for fabricating gated single crystalline silicon (c-Si) field emitter arrays. His method became a kind of standard for fabricating Si FEAs, and a lot of variations were investigated. Here, the fabrication is explained along with Fig. 1. First, a silicon dioxide disc-shaped mask is formed by thermal oxidation, photolithography, and reactive ion etching (RIE) (a). Then, single crystalline silicon is etched through the SiO_2 disc by RIE to form a tip structure (b). The RIE ends before the SiO_2 mask is removed and then sharpened by using thermal oxidation (c). A moderate thermal oxidation temperature about 950° C can sharpen the tip. After the sharpening, the insulator SiO_2 and gate metal

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are deposited by using an evaporator (d). A self-aligned gate aperture is formed in this step. The overlying structure on the emitter tip is removed by using a buffered hydrofluoric (BHF) acid solution (e). Fig. 1(f) shows a silicon emitter with Nb gate electrode fabricated by the authors referring to Betsui's method. The merits of this process are that a very sharp tip can be obtained uniformly by using thermal oxidation, which was confirmed by TEM observation [15], and that the gate aperture is self-aligned.

2.2. Polycrystalline silicon, amorphous silicon, sharpening

The polycrystalline silicon (poly-Si) emitter is investigated in order to lower the fabrication cost and to overcome the limitation of the substrate size especially in the field of the field emission display [16–19]. The basic fabrication procedure is similar to that of c-Si FEAs from the viewpoint of using isotropic etching by RIE and thermal oxidation sharpening. However, poly-Si FEAs have a rough tip structure and asymmetric gate aperture due to the grain boundary. The rough morphology of the tip and gate structure causes the increase of the undesired gate current. The large gate current is apt to cause tip and gate disruptions due to an arc discharge between the tip and gate electrode [20]. Hence, poly-Si FEA has difficulties in uniformity, reliability and stability. Using amorphous Si (a-Si) is an alternate for overcoming the substrate limitation problem. In this case thermal oxidation sharpening cannot be applied because of the significant damage done to the a-Si surface morphology. An alternative sharpening process was developed by using ion etching [21]. Two-step ion etching using Ar and CHF_3 reactive ion etching (RIE) is applied at room temperature. A starting emitter tip, which is fabricated out of amorphous silicon (a-Si) with RIE of an SF_6 and O_2 gas mixture, has the shape of a circular truncated cone whose top is flat. Ar ion etching sharpens the apex of the emitter moderately. However, the tip is still blunt. CHF_3 RIE after Ar ion etching shapes the emitter tip into a cone with a much sharper apex. An interesting point is that sharpening does not occur by CHF_3 RIE only. The combination of Ar sputtering and CHF_3 RIE makes the very sharp tip, even at room temperature. This low temperature process is applicable for display applications that use a glass substrate.

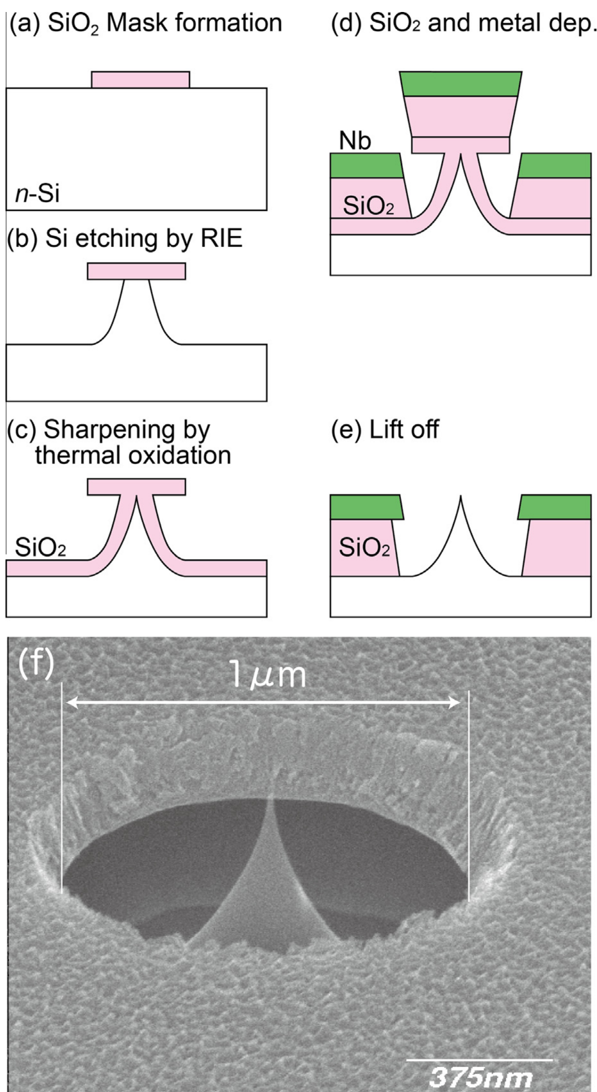

Fig. 1. Procedure for fabricating gated silicon field emitter by thermal oxidation sharpening [14] and SEM image of the fabricated emitter.

2.3. Etch-back method for gate formation

In the fabrication with Betsui's method, the lift-off process for the metal disc [step (d) in Fig. 1] is a kind of bottleneck to improving the fabrication yield because the small metal disc becomes a waste particle and causes a short problem between the tip and gate. In addition to this, the initial SiO_2 mask determines the diameter of the gate aperture; therefore, we cannot miniaturize the gate aperture with an additional process in order to improve the emission characteristics. The etch-back method is another solution for making the gate aperture [22–24]. Fig. 2 is a typical procedure of the etch-back method. The starting point is just after the emitter tip formation shown in Fig. 1(c). After this formation, SiO_2 is removed by BHF, and then, the gate insulator SiO_2 and gate metal are deposited by PE-CVD and sputtering, respectively (a). Note that the material that is not affected by BHF should be selected as a gate

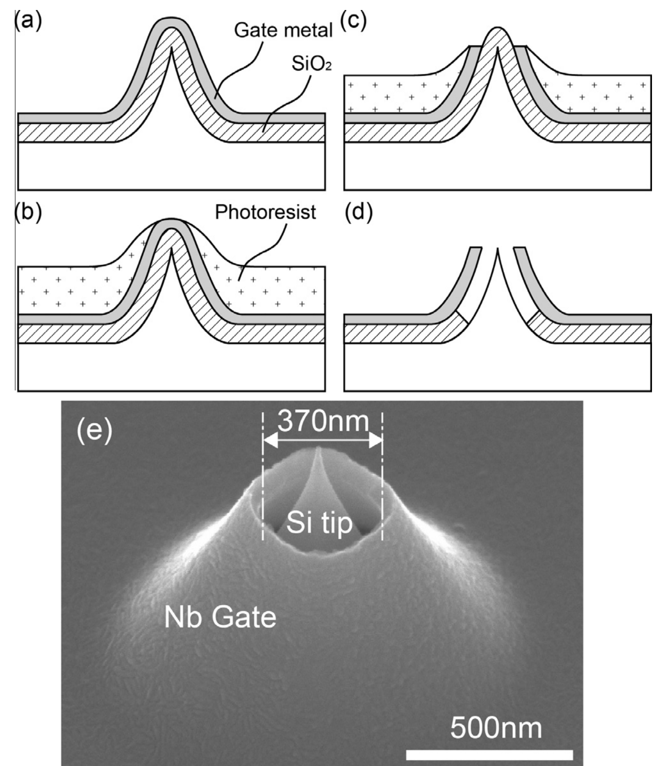

Fig. 2. Etch-back method for making gate aperture on silicon emitter cone and SEM image.

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