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Review Article

Low-power-consumption fully depleted silicon-on-insulator technology

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ABSTRACT

Scaling the CMOS device has continuously improved its functionality and performance while lowering its power consumption and price. However, the current "scaled CMOS" technology faces several problems regarding power consumption, and a migration to new transistor structures is proceeding. "Fully depleted silicon on insulator" (FDSOI) technology can lower power consumption and improve performance of CMOS circuits with a capability of low-voltage operation. This article reviews advances in FDSOI technology: device structure, back-bias control function, fabrication process, demonstration of small variability of transistors, reliability including soft error, low voltage circuit design and silicon verification, and improvement in the energy efficiency of CMOS logic circuits. The strong requirement of further improvement in energy in the near future is finally pointed out.

1. Introduction

Continuous development of the semiconductor industry has derived by the advancement in CMOS transistor technology, as well as circuit and system design with electronic design tools, and manufacturing technology including materials and equipments. This advancement has been mainly relying on the scaling down of transistors that has been continuing for about forty years since the scaling concept was first proposed in 1974 by Dennard [1]. According to this concept, that is, the "ideal scaling rule," the number of transistors on a chip increases at a rate of about two times per generation corresponding to shrinking transistor size about 0.7 times. At the same time, other parameters (such as voltage and capacitance) continuously decrease at the same rate as transistor size, and the functionality and operating speed of the CMOS circuits continue to increase without increasing the power consumption of a chip.

Current CMOS technology, however, is facing many problems regarding the physical limitation that hinders transistor miniaturization based on the ideal scaling rule. Increasing power consumption of a chip is one significant problem. The operating (active) power consumption per unit CMOS circuit is higher than the value expected in the ideal-scaling framework because of a retarded voltage down-scaling. Increasing the standby (leakage) power is also a serious problem because the scaling down of transistor size to nearly nanometer level increases leakage current (which is related to tunneling) everywhere in the transistor. Moreover, the short-channel effect (SCE) deteriorates the cutoff characteristics of transistors.

The continuing development of information and communication technology has been increasing the total power consumption of electronic devices worldwide. The increasing number of smartphones and the advent of the "Internet of Things" (IoT) era will further increase the power consumption. Low power and high energy efficiency in regard to both design and manufacturing have become more significant factors in the future CMOS technology. In past years, low-power CMOS technology was mostly aimed at mobile devices. However, enterprise systems (such as servers and network appliances) should be more energy conscious than they were in the past because the total amount of data is increasing exponentially. In the IoT era, the number of tiny electronics (like sensors) will also increase exponentially and exceed the trillion level by the year 2020 [2]. These tiny electronics, ideally, should work on a self-powered basis (a zero sum between energy generation and consumption). The power-saving approaches for these two cases, enterprise systems and tiny electronics, will be slightly different, though their efficiencies should be maximized by both approaches within the limited quantity of available electric power. In this paper, "fully depleted silicon on insulator" (FDSOI) technology, which is mainly aimed at low-power consumption and high energy efficiency, is reviewed. There are several textbooks relating to the contents of this paper available [3–6] for further information.

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2. FDSOI technology

2.1. What is FDSOI?

The essence of the Dennard's scaling rule is to minimize the size of transistors (which affects the number of transistors crammed onto a chip) in the vertical direction as well as in the horizontal direction. In the case of conventional bulk transistors, the vertical scaling is done by narrowing the depletion length of both the channel and the source/drain regions by increasing the impurity density of silicon in those regions. In the case of current scaled transistors, scaling in this manner poses problems such as increasing tunnel leakage current through the very narrow depletion layer and increasing statistical variability (which will be described later in this paper).

The FDSOI transistor is particularly suited for the current scaled CMOS technology. "SOI" means the structure of the transistor or the substrate that the top silicon layer (channel layer or silicon body) is placed on the insulator layer named buried oxide (BOX) layer on top the silicon base wafer. The SOI transistor basically includes two types of structures: partially depleted SOI (PDSOI) and FDSOI. The difference between these two structures is the thickness of the top silicon, that is, the SOI layer. In case of PDSOI, the depletion length (which is determined by the impurity density of the SOI layer) is thinner than the SOI layer thickness and, hence, partially depleted. The scaling in the vertical direction is done by increasing the impurity density in the same manner as bulk transistors. On the other hand, in the case of FDSOI, the SOI layer is fully depleted, and the vertical scaling is simply done by thinning the SOI layer. As for normal operation of the scaled FDSOI transistor, impurity doping in the SOI layer is not needed, and the short-channel effect is controlled by the SOI layer thickness itself.

2.2. Single- and double-gate FDSOI

The number of gate electrodes facing the channel of a transistor significantly affects the characteristics of the transistor. Roughly speaking, increasing the number of gates improves SCE immunity because the electrostatic control integrity by the gate electrode becomes better with increasing gate number [4,5]. The FDSOI transistor has a planar structure similar to that of a bulk transistor. The double-gate-like action is possible if the BOX layer is sufficiently thin and an additional (bottom) gate electrode is placed under the BOX layer. The insertion of a bottom-gate electrode usually requires very complicated and difficult process technology and has never been commercially used. Instead, impurity doping in the region of the silicon base wafer just under the BOX layer makes the double-gate-like action possible. This doping region is called the "ground plane" (GP). With a terminal contacting the GP region, the back-gate bias voltage can be applied to control the transistor characteristics. The structural differences among the above-described transistors are illustrated in Fig. 1.

2.3. History of FDSOI technology development

Research and development on FDSOI started in the late 1980s [7,8]. At that time, the quality of the substrates was problematic (that is, defect density was high) because they were fabricated by oxygen implantation [9]. Commercial-based developments of SOI technologies were triggered by the development of high-quality SOI substrates with thin top silicon layers. Both ELTRAN [10] and UNIBOND [11] have highly controllable thicknesses of both SOI and BOX layers as well as low defect density. From the viewpoint of device physics, decreasing operating voltage of CMOS circuits to less than 2 V by CMOS scaling made it possible to implement FDSOI because the maximum operating voltage determined by the parasitic bipolar action is roughly less than 2 V. The first commercial product based on FDSOI CMOS was released by Oki Electric [12] as an application in a solar-powered watch.

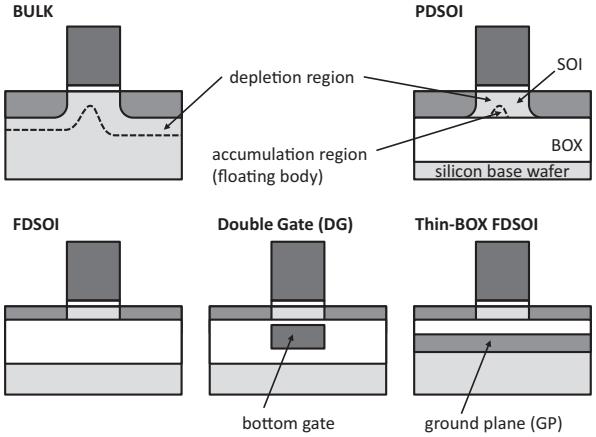

Fig. 1. Schematic structures of bulk, PDSOI, FDSOI, DG, and GP transistors.

The concept of the double-gate transistor was first disclosed in 1984 [13]. A double-gate-like structure with a thin BOX layer and a doped GP was proposed in 1988 [14]. The concept of FDSOI capable of back-gate bias control with a thin BOX layer, named "silicon on thin buried oxide" (SOTB), was first proposed in 2004 [15]. These structures are compared in Figs. 2 and 3. Although they look very similar, their manufacturabilities are different. Synchronizing the development of a high-quality SOI substrate, especially the commercial availability of a thin-BOX type SOI substrate, SOTB has become a structure that is easy to fabricate with current CMOS manufacturing technology. Research and development on this structure and related ones has been continued over recent years by Renesas, LEAP, CEA-Leti, STMicroelectronics, IBM, and others. STMicroelectronics recently released a commercial FDSOI chip based on 28-nm technology. In the following sections, the technology of FDSOI devices with a thin BOX layer is mainly described.

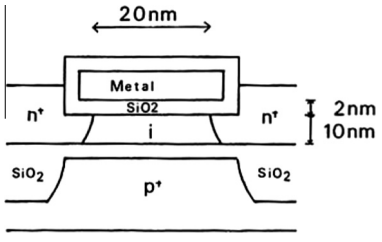

Fig. 2. Ultimate scaled-down nMOSFET [14] ©JSAP.

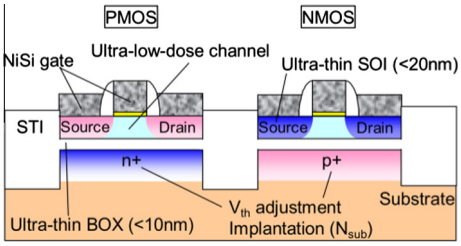

Fig. 3. Structure of silicon-on-thin-BOX transistor [15] ©IEEE.