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Review Article

A technological and electrical study of self-aligned charge-trap split-gate memory devices

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ABSTRACT

In this work, self-aligned charge trap split-gate devices with memory gate lengths down to 16 nm and select gate lengths down to 30 nm are fabricated and studied. Main technological issues are addressed. We present the impact of charge-trap layer (SiN or Si-nc), of memory gate length and also of spacer memory shape on electrical results (programming window). We show functionality of ultra-scaled devices, with good programming and erasing performances.

1. Introduction

Due to the increasing demand for consumer, industrial and automotive products, low-power, fast speed and highly reliable embedded memories are required. Split-gate flash memories can meet all these requirements. Different approaches can be found in the literature, using either silicon nitride (Si_3N_4) [1] or silicon nanocrystal (Si-nc) [2,3] as charge trapping layer. A comparative study had been previously presented between Si_3N_4 and Si-nc based ultra-scaled – split-gate memories in which the memory gate was fabricated by using lithography [4]. Nevertheless, such an approach could suffer from some drawbacks, in terms of reliability and variability, linked to the lithography misalignment between the select gate and the memory gate. In this paper, self-aligned architectures, in which the memory gate is a poly-Si spacer, are studied; we evaluate the impact of three parameters on the memory window: nature of charge trapping layer, memory gate length as well as the memory gate spacer shape.

2. Split-gate fabrication

2.1. Technological details

Split-gate charge trapped memories were fabricated with a "memory last" configuration, in which the select gate (SG) is processed first (deposited and patterned), and the memory gate (MG) is then deposited.

Fig. 1 shows previously presented split-gate charge-trap memories (called integration 1) where the memory gate is fabricated by using lithography [4]. The electrical memory gate length (L_{MG}) was controlled by the poly-Si layer overlapping the memory channel (Fig. 1), allowing to achieve very low gate lengths, down to 20 nm [4]. But the use of lithography induces a misalignment between the select gate and the memory gate, implying a strong variation of the memory gate length and so a strong variation of the electrical performances, such as the memory window.

We present here a second approach (called integration 2), in which the memory gate is a poly-Si "spacer" formed on the sidewall of the select transistor. This allows to avoid costly lithography steps, and solve the misalignment issue (Fig. 2). Memory gates were fabricated with lengths down to 16 nm.

Either Si_3N_4 or hybrid Si-nc/SiN charge trapping layers were used for both architectures 1 and 2 presented before (see Figs. 1 and 2).

The main challenge concerns the precise control of the spacer memory gate shape and of the memory gate length. Spacer gate has to fulfil two tricky requirements: being as flat as possible in order to get a silicidation surface as large as possible and insure a functional contact (see area 1, Fig. 3) and getting a steep edge (see area 2, Fig. 3) in order to control the drain junction doping.

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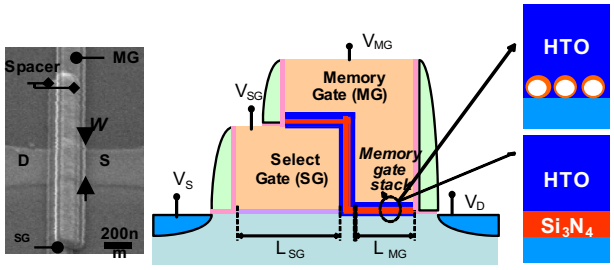

Fig. 1. SEM plane view of channel, select gate and memory gate (left), and schematic cross section of a split-gate memory in which the MG is processed by lithography (right) [4].

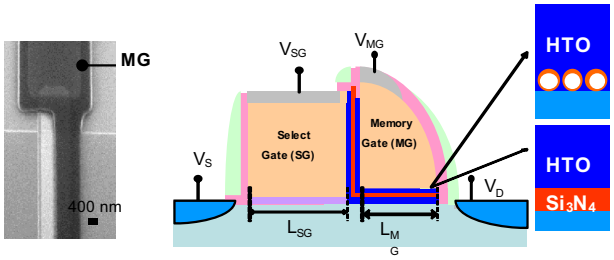

Fig. 2. SEM plane view of select gate and memory gate (left), and schematic cross section of a split-gate memory in which the memory gate is processed as a spacer (right).

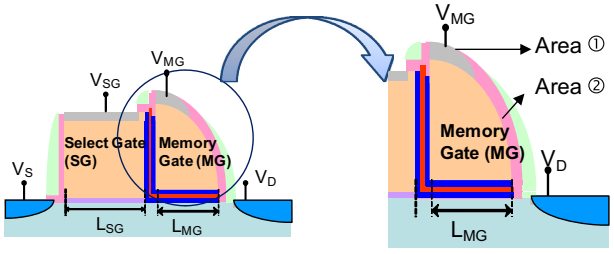

Fig. 3. Enlargement of the spacer memory gate.

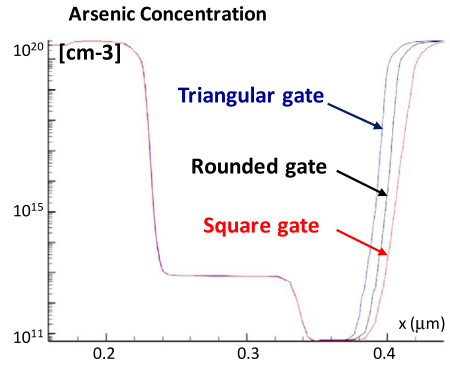

Fig. 5. Bottom right: evolution of arsenic active concentration along a horizontal line situated 1 nm under the surface of the channel.

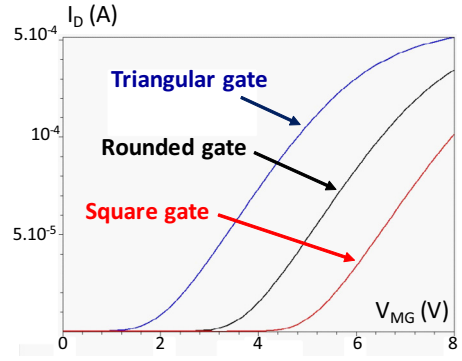

Fig. 6. Evolution of drain current (I_D) as a function of memory gate voltage (V_{MG}) for the 3 spacer forms. Select gate voltage = V_{SG} = 1.5 V, V_S = 0 V, V_D = 5 V. L_{SG} = 100 nm, L_{MG} = 50 nm.

2.2. Spacer memory shape: simulations and fabrication

Simulations were performed by using Sentaurus Process TCAD software in order to evaluate the influence of the spacer geometry on drain junction [refSyn1]. Three different spacer shapes were

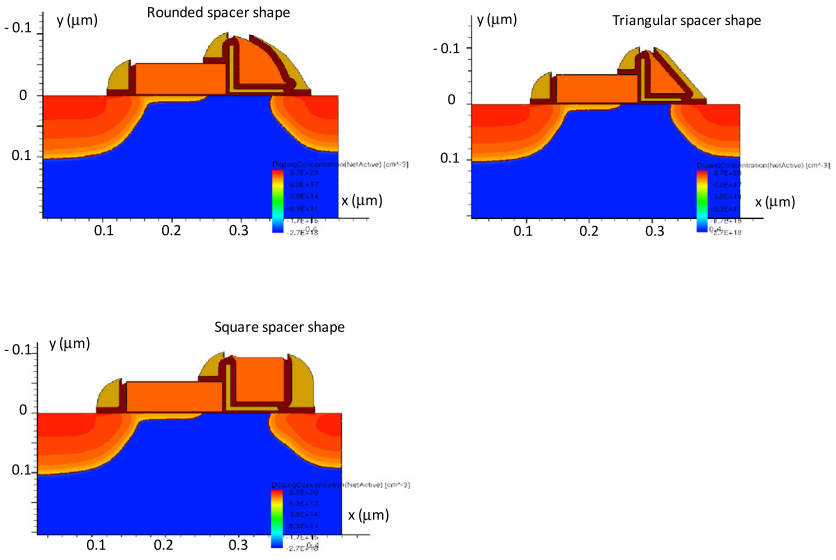

Fig. 4. Simulations performed with 3 different spacer shapes. Top left: rounded spacer. Top right: triangular spacer shape. Bottom left: square spacer shape.