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# Fully CMOS-compatible top-down fabrication of sub-50 nm silicon nanowire sensing devices

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A B S T R A C T

This article reports the fabrication of sub-50 nm field effect transistor (FET)-type silicon (Si) nanowire (Si NW) chemical and biological sensing devices with a junctionless architecture, as well as on the initial characterisation of their electrical and sensing performance.

The devices were fabricated using a fully complementary metal-oxide-semiconductor (CMOS)-compatible top-down process on silicon-on-insulator (SOI) wafers. The fabrication process was mainly based on high-resolution electron beam lithography (EBL) and reactive ion etching (RIE) but also included photolithography (mix-and-match lithography), thin film deposition by electron beam evaporation, lift-off, thermal annealing and wet etching.

The sensing performance of a matrix of nanowire devices, i.e. containing 1, 3 and 20 NWs with lengths of 0.5, 1 and 10 μm was examined. Each element of the matrix also contained five devices with different NW widths: 10, 20, 30, and 50 nm and 5 μm (a Si belt reference device). Electrical characterisation of the devices showed excellent performance as backgated junctionless nanowire transistors (JNTs): high on-currents in the range of 1–10 μA and high ratios between the on-state and off-state currents ($I_{on}/I_{off}$) of 6–7 orders of magnitude. In addition, the results of ionic strength sensing experiments demonstrate the very good sensing capabilities of these devices. To the best of our knowledge, these nanowire sensors are among the smallest top-down fabricated Si NW devices reported to date.

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## 1. Introduction

Si nanowires (Si NWs) have received significant academic and commercial attention due to their attractive electrical and mechanical properties and large surface area to volume ratios. Such materials are promising as channels for field effect transistors (FETs) [1] and also as sensing devices [2,3]. Initially, FET-type nanowire sensors were fabricated using grown NWs [2]. Whilst Si NWs can be produced in reasonable quantities from 'bottom-up' synthetic methods, their post positioning and alignment remains a challenge. Issues associated with nanowire alignment are overcome by producing arrays of nanowires from 'top-down' methodologies, e.g. electron beam lithography (EBL). Lithography also allows better control over nanowire geometries, i.e. control over length, width, thickness, number and orientation along different Si crystallographic axes. These parameters are particularly important for sensing applications and have been theoretically [4] and to some extent, experimentally investigated [5,6]. However, to the best of our knowledge, there has been no consistent experimental study of their influence on the electrical and sensing performance of sub-50 nm Si NWs.

Here we report the top-down fabrication of a range of Si NW sensing devices having various nanowire densities, lengths and widths. The operation of these devices relies on the principle of a field effect transistor. In contrast to most sensors of this type, however, our devices have a junctionless architecture [7–9], i.e. the source, channel (nanowires) and drain have the same dopant polarity (*p*-type in this case) without any junctions between them. Such devices are easier to fabricate than the traditional FETs since

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they do not require separate doping of the source and drain regions. They also possess a number of other advantages over the conventional inversion-mode FETs [7–9].

The devices were fabricated mainly by electron beam lithography and reactive ion etching (RIE) on silicon-on-insulator (SOI) wafers. For every single die of the wafers, a matrix of three different nanowire densities (1, 3, and 20 NWs) and lengths (0.5, 1, and 10 μm) was designed, making nine elements altogether. Each element of the matrix contained five devices with different NW widths: 10, 20, 30, and 50 nm and 5 μm (a Si belt reference device), permitting 45 different devices on a chip (see Fig. 1). The initial electrical characterisation of the devices revealed well-functioning backgated junctionless nanowire transistors (JNTs). In addition, the data obtained from ionic strength sensing experiments demonstrate their very good sensing performance.

## 2. Materials and methods

SOI wafers with a lightly *p*-doped top Si layer of 70 nm, a buried oxide (BOX) $SiO_2$ layer of 145 nm and a lightly *p*-doped base Si layer of 500 μm (Soitec) were used in this study.

The top device layer of the SOI wafers was oxidised, via dry thermal oxidation, to form a thin 45 nm $SiO_2$ layer. As a result, the thickness of the device layer was reduced from 70 to 44 nm prior to doping with boron (B) by ion implantation to a dose of $4 \times 10^{13}$ cm$^{-2}$ at ion energy of 14 keV and a tilt angle of 7°. The implantation conditions are selected in such a way as to position the peak of implanted ion depth distribution within the top Si layer. In this way, high doping efficiency with minimum implantation damage and minimum number of implanted ions outside the top Si layer are achieved. Dopant activation was attained by furnace annealing at 900 °C for 30 min in a nitrogen environment. The effective doping concentration in the Si device layer was estimated to be equivalent to $\sim 1 \times 10^{18}$ cm$^{-3}$.

Two EBL exposures were undertaken on a full 4'' SOI wafer using a JEOL JBX 6000FS Gaussian beam direct write system operated at 50 kV. In the first exposure, alignment marks were defined in a 425 nm thick layer of ZEP520A positive resist (Nippon ZEON Corp.), using the low-resolution high-current mode of the system. The marks were etched 1.5 μm deep through the ZEP mask with a two-stage plasma etching process. Subsequently the resist was removed and the top $SiO_2$ layer wet etched in 10:1 buffered oxide etchant (BOE), resulting in a Si device layer thickness of 44 nm. The thickness variation was measured to be 0.4 nm across a 4'' wafer.

In the second EBL exposure, the nanowire devices (nanowires together with the source and drain contact pads) were defined in a 50 nm thick layer of hydrogen silsesquioxane (HSQ) negative tone resist (XR-1541 from Dow Corning Corp.), using the high-resolution mode of the system and a beam current of 100 pA. In order to ensure definition of resist structures down to 10 nm, as well as full CMOS compatibility of the fabrication, an original high-contrast and low roughness development process, using 25% tetramethylammonium hydroxide (TMAH) as the main step [10,11], was implemented. The widely used HSQ salty developer NaOH (1 wt%)/NaCl (4 wt%) [12] was wittingly avoided since sodium is an unwanted impurity in CMOS devices [13] and wafer processing with this developer would not be allowed in our CMOS compatible Si Fab.

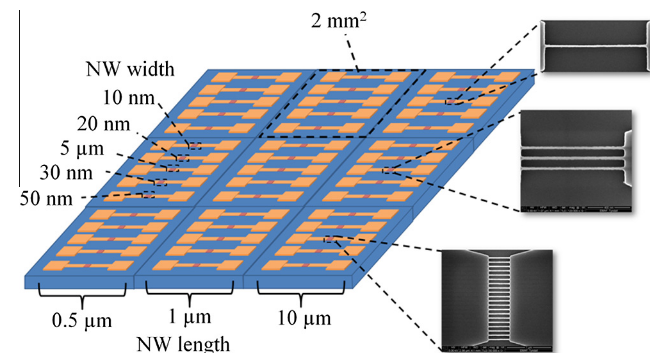


**Fig. 1.** Overview of the design layout.

To transfer the HSQ lithographic pattern into the top Si layer, RIE processing with chlorine (Cl) chemistry in a Plasmalab System 100 from Oxford Instruments was used. Subsequently, an additional 200 nm $SiO_2$ layer was deposited on the whole surface, except the device regions, to minimise the leakage current through the buried oxide. This deposition was done by electron beam evaporation in Leybold Lab 600 system and was combined with photolithography and lift-off to clear the oxide from the device regions. Next, the HSQ resist was removed and metal contacts and interconnection were created by electron beam evaporation (Temescal FC-2000) of a stack of 100 nm platinum (Pt) and 40 nm nickel (Ni) layers and the respective photolithography and lift-off steps. Then, a passivation layer of 500 nm $SiO_2$ was deposited again on the whole surface, except the device regions and metal pads. This deposition was also done by electron beam evaporation (Leybold Lab 600) and combined with photolithography and lift-off to clear the oxide from the device regions and the metal pads. All photolithography exposures were aligned to the previously exposed EBL pattern using the etched alignment marks, i.e. mix-and-match lithography was undertaken. To improve the conductivity of the devices, they were thermally annealed for 30 min at 425 °C in forming gas (10% $H_2$/90% $N_2$). The complete processing of the wafers is summarised in the following process flow:

- Oxidation of the top Si device layer,
- Boron (B) doping by ion implantation,
- Dopant activation by furnace annealing,
- Electron beam lithography (EBL) of the alignment marks,
- Plasma etching of the alignment marks,
- Wet etching of the top $SiO_2$ layer,
- Second EBL exposure (high resolution) of the nanowire devices,
- Reactive ion etching of the nanowire devices,
- Photolithography,
- Deposition of an additional $SiO_2$ layer by electron beam evaporation,
- Lift-off,
- Photolithography,
- Removal of the HSQ electron beam resist,
- Metal deposition by electron beam evaporation,
- Lift-off,
- Photolithography,
- Deposition of an $SiO_2$ passivation layer by electron beam evaporation,
- Lift-off,
- Forming gas anneal.

A cross-section of fabricated devices is schematically presented in Fig. 2.

Electrical characterisation of the devices, as well as the ionic strength sensing experiments was performed using a cascade manual probe station and Agilent semiconductor analyser B1500.

In order to demonstrate the sensing capabilities of our devices, ionic strength sensing experiments were performed. In these experiments, solutions of different ionic strengths but equivalent pH values were generated by diluting phthalate buffered solution (Fisher, pH 7) with deionised (DI) water (pH 6.8). To make a 5× diluted solution (dilution 1), 2.0 ml of the buffer was measured

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