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Electrically active interface defects in the $In_{0.53}Ga_{0.47}As$ MOS system

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ABSTRACT

In this work we present experimental results examining the energy distribution of the relatively high ($>1 \times 10^{12}$ cm^{-2} eV^{-1}) density of electrically active defects which are commonly reported at the interface between high dielectric constant (high-*k*) thin films and $In_{0.53}Ga_{0.47}As$. The interface state distribution is examined for the $Al_2O_3/In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor (MOS) system based on analysis of the full gate capacitance (C_g–V_g) of the surface *n*-channel $In_{0.53}Ga_{0.47}As$ MOS transistors. The experimental capacitance, recorded at −50 °C and 1 MHz to approximate a high frequency response, is compared to the theoretical C_g–V_g response to evaluate the interface state distribution across the $In_{0.53}Ga_{0.47}As$ energy gap and extending into the $In_{0.53}Ga_{0.47}As$ conduction band. To improve the accuracy of the fitting process, the Maserjian Y-function was used in the modeling of the interface defects and fixed oxide charge densities. The analysis reveals a peak of donor-like interface traps with a density of 1.5×10^{13} cm^{-2} eV^{-1} located at ~0.36 eV above the $In_{0.53}Ga_{0.47}As$ valence band edge, a high density of donor-like states increasing towards the $In_{0.53}Ga_{0.47}As$ valence band. The analysis also indicates acceptor-like interface traps located in the $In_{0.53}Ga_{0.47}As$ conduction band, with a density of $\sim 2.5 \times 10^{13}$ cm^{-2} eV^{-1} at 0.3 eV above the $In_{0.53}Ga_{0.47}As$ conduction band minima. The reported interface state density is similar to reports for others oxides, suggesting that the recorded interface states originate from the $In_{0.53}Ga_{0.47}As$ surface.

1. Introduction

For several decades improvements in the performance of integrated circuits (IC's) has been based primarily on transistor miniaturisation. However, as minimum device dimensions reduced to below 50 nm, transistor miniaturisation no longer remained as the single driving force behind the development of nano-electronic integrated circuits. In recent technology generations new materials have been incorporated into the device to enhance transistor performance and to maintain or reduce the overall power dissipation of integrated circuits. High dielectric constant (high-*k*) materials have been introduced into the gate stack to minimise gate leakage current while maintaining capacitive coupling between the gate and the channel [1]. New device architectures have been implemented to induce strain into the transistor in order to boost the carrier mobility in the channel [2]. Looking beyond the 22 nm technology node, there is a strong research interest in the heterogeneous integration onto a silicon platform of high mobility semiconductors, such as germanium [3] or GaSb [4] for *p* channel devices, and III–V compound semiconductors for the complementary *n* channel devices.

Considering the *n* channel devices, many III–V substrate options have been reported, including, GaAs [5], $In_xGa_{1-x}As$ [6,7], InAs [8] and InSb [9]. Indeed, the viability of using such high mobility materials has recently been given a new impetus for a number of reasons. Firstly, there has been significant progress in the integration of III–V materials onto a silicon platform [6,10]. Secondly, the use of atomic layer deposition [11] has been shown to lead to considerable improvements in the electronic properties of the high-*k*/III–V interface and the demonstration of true inversion in $In_{0.53}Ga_{0.47}As$ MOS systems [12–14]. Thirdly, there have been very encouraging recent results indicating specific contact resistivity values to III–V compounds as low as $\sim 2 \times 10^{-9}\ \Omega$ cm^2 [15]. The combination of these three factors has revitalised the interest in III–V materials for high performance and low power *n* channel device applications.

For the successful incorporation of these alternative III–V channels into future MOSFET processes it is required to both quantify and control electrically active interface state defect densities (D_{it}) which are present at the high-*k*/semiconductor interface as well as fixed charges and electron or hole traps which are located within the high-*k* oxide layer. Considering the case of the high-*k*/$In_{0.53}Ga_{0.47}As$ MOS system, interface state densities at around the mid-gap energy in the $In_{0.53}Ga_{0.47}As$ energy gap are

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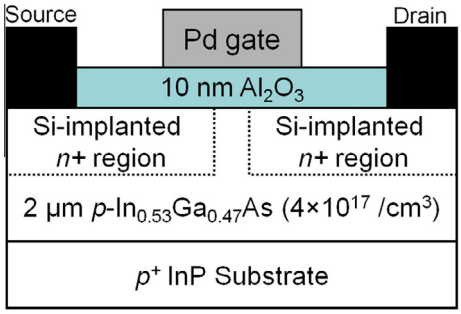

Fig. 1a. Schematic cross-sectional diagram of a surface-channel $In_{0.53}Ga_{0.47}As$ MOSFET with a 10-nm thick ALD Al_2O_3 gate dielectric.

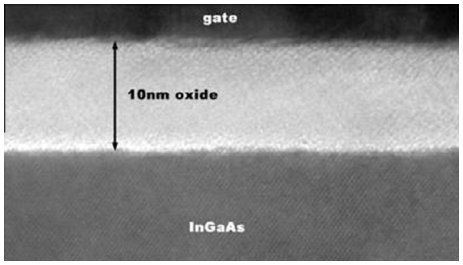

Fig. 1b. Cross sectional TEM images through the gate stack region of the MOSFET. A C_{OX} of 7.6 × 10^{-3} F/m^2 was obtained based on the extracted Al_2O_3 *k*-value of 8.6 and the measured T_{OX} of 10 nm.

typically reported to be in the range mid-10^{12}–$10^{13}$$cm^{-2}$ eV^{-1} [16–19]. These densities remain too high for practical device applications. As well as the density of interface defect states at the mid-gap energy region, it is important to characterise the distribution of interface defects throughout the energy gap, referred to here as $D_{it}(E)$. Knowledge of $D_{it}(E)$ is important as any specific features in the density of interface states distribution can be compared to theoretical models of defect energies [20] as a method to identify the physical origin of the interface states.

One approach to obtain the distribution of interface states across the band gap in the high-*k*/$In_{0.53}Ga_{0.47}As$ MOS system is to obtain the true quasi-static CV response, and obtain $D_{it}(E)$ by a comparison to the theoretical response [21]. An alternative approach is to use both *n* and *p* type $In_{0.53}Ga_{0.47}As$ MOS structures to examine $D_{it}(E)$ in the upper and lower portions of the $In_{0.53}Ga_{0.47}As$ energy gap [22]. Ali et al. [23] reported a method to determine the $D_{it}(E)$ across the energy gap based on the frequency dependent gate to channel capacitance and conductance of an surface channel $In_{0.53}Ga_{0.47}As$ MOSFET. In this work we extend on these studies to explore the use of the full gate capacitance of an $In_{0.53}Ga_{0.47}As$ surface *n*-channel MOSFETs, in conjunction with the Maserjian Y-function, to profile the interface state density across the gap. The results are compared to other reports in the literature.

2. Sample details

The experimental samples used in this study to investigate the interface state density profile are surface-channel MOSFETs fabricated on a 2-μm-thick Zn-doped (4×10^{17} cm^3) *p*-$In_{0.53}Ga_{0.47}As$ layer grown on a 2-inch *p* + InP wafer by metal-organic vapor phase epitaxy (MOVPE). The $In_{0.53}Ga_{0.47}As$ surface passivation prior to gate oxide deposition was an immersion in 10% $(NH_4)_2S$ at room temperature for 20 min, which was found to be an optimum in terms of interface state reduction and for the suppression of native oxide formation [22], [24]. The transfer time to the atomic layer deposition (ALD) reactor after surface passivation was less than 5 min. A 10-nm-thick Al_2O_3 gate oxide film was formed by ALD using alternating pulses of $Al(CH_3)_3$ (TMA) and H_2O precursors at 250 °C. The source and drain (S/D) regions were selectively implanted with a Si dose of 1×10^{14} cm^2 at 80 keV and 1×10^{14} cm^2 at 30 keV. Implant activation was achieved by rapid thermal anneal (RTA) at 600 °C for 15 s in a N_2 atmosphere [25]. A 140-nm-thick SiO_2 field oxide was formed by electron beam evaporation and lift-off to minimize the gate pad capacitance. A 200-nm-thick Pd gate was defined by electron beam evaporation and lift-off. Non-self-aligned ohmic contacts were defined by lithography, selective wet etching of the Al_2O_3 in dilute HF and electron beam evaporation of an Au (14 nm)/Ge (14 nm)/Au (14 nm)/Ni (11 nm)/Au (200 nm) metal stack [26]. A 300 °C for 30 min forming gas (5% H_2/95% N_2) anneal was carried out in an open tube furnace. A schematic cross section of the device is shown in Fig. 1a, with a TEM image of the gate stack region presented in Fig. 1b, confirming the thickness of the ALD formed Al_2O_3 layer as 10 nm. The surface-channel $In_{0.53}Ga_{0.47}As$ *n*-MOSFETs, featured a threshold voltage, V_T, of 0.43 V, an inverse subthreshold slope, SS, of 150 mV/dec., an I_{ON}/I_{OFF} of ~10^4 and a source/drain resistance, R_{SD}, of 103 Ω, Further details can be found in [27].

3. Experimental results

3.1. Full gate capacitance of the $In_{0.53}Ga_{0.47}As$ MOSFET: Evaluation of the integrated D_{it}

The full gate capacitance of the $In_{0.53}Ga_{0.47}As$ MOSFET as a function of the applied gate voltage (C_g–V_g) characteristic was obtained using a measurement configuration with the gate contact connected to the "high" of the impedance meter and the source, drain and substrate contacts shorted together and connected to the "low". In this measurement configuration the inversion charge is provided through the source and drain for the condition of strong inversion at the Al_2O_3/*p*-$In_{0.53}Ga_{0.47}As$ interface, and the full C_g–V_g response can be obtained [28].

Fig. 2 shows an example of the full gate capacitance of the *n* channel MOSFET (W = 100 μm, L = 10 μm) measured at 20 °C from 1 kHz to 1 MHz. The experimental C_g–V_g characteristic was corrected for parasitic capacitances using the method reported in

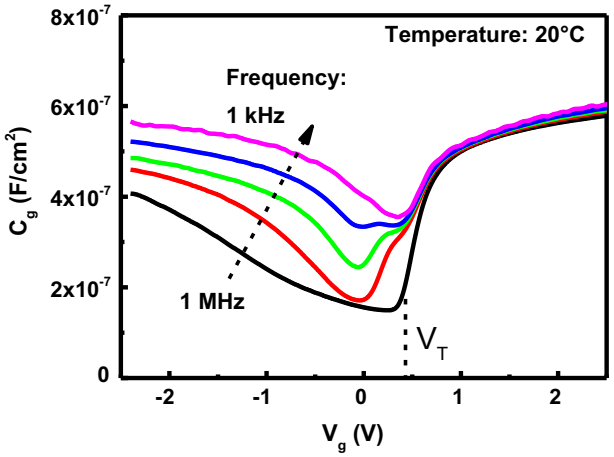

Fig. 2. The multi-frequency gate capacitance (C_g–V_g) response of an *n*-channel $In_{0.53}Ga_{0.47}As$ MOSFET recorded at room temperature for selected frequencies (1 kHz to 1 MHz). The C_g–V_g response was measured with the gate contact connected to the "high" of the impedance meter and the source, drain and substrate contacts shorted together and connected to the "low".