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Superior reliability of high mobility (Si)Ge channel pMOSFETs

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ABSTRACT

With a significantly reduced Negative Bias Temperature Instability (NBTI), SiGe channel pMOSFETs promise to virtually eliminate this reliability issue for ultra-thin EOT devices. The intrinsically superior NBTI robustness of the MOS system consisting of a Ge-based channel and of a SiO_2/HfO_2 dielectric stack is understood in terms of a favorable energy decoupling between the SiGe channel and the gate dielectric defects. Thanks to this effect, a significantly reduced time-dependent variability of nanoscale devices is also observed. Other reliability mechanisms such as low-frequency noise, channel hot carriers, and time-dependent dielectric breakdown are shown not to be showstoppers.

1. Introduction

Due to the ever increasing electric fields in scaled CMOS devices, reliability is becoming a showstopper for further scaled technology nodes. Although several groups have already demonstrated functional devices with aggressively scaled EOT down to ~5 Å [1,2], the stability of their parameters at operating conditions cannot be guaranteed [3,4]. Meanwhile, the use of high-mobility channels is being considered for further device performance enhancement in future CMOS technology nodes [5,6]. The SiGe channel quantum well technology (Fig. 1) in particular is considered for yielding enhanced mobility and pMOS threshold voltage tuning [7].

While the interface passivation of non-Si channel materials is typically considered a challenging and critical issue, extremely promising device performance was recently obtained by growing epitaxially a thin Si passivation layer on top of a pMOS (Si)Ge channel [8]. However, open questions exist about the reliability of such complex gate stacks.

In this paper we review our recent studies regarding the reliability of Ge-based pMOSFETs. We show that this technology offers a significant intrinsic reliability improvement which we ascribe chiefly to a reduced interaction between channel carriers and oxide defects. Furthermore, we show that the (Si)Ge-based technology also considerably alleviates the time-dependent variability [9], which arises as devices scale toward atomistic dimensions [10]. The extensive experimental results summarized here strongly support (Si)Ge pMOS technology as a clear frontrunner for future CMOS technology nodes.

2. Negative bias temperature instability

Negative Bias Temperature Instability (NBTI) is considered as the most severe reliability issue for scaled CMOS technologies [11,12]. It affects pMOSFETs during operation, causing significant shifts of the device electrical parameters (e.g., threshold voltage shift ΔV_{th}) due to oxide defect charging and interface state creation. The quasi-constant supply voltage scaling proposed by the international technology road map [13] for the recent and upcoming technology nodes enhances NBTI due to the ever increasing oxide electric field (E_{ox}) [14]. As a consequence, a 10 year lifetime at operating conditions cannot be guaranteed anymore for Si channel pMOSFETs with ultra-thin (UT-) EOT (Fig. 2 diamonds).

Already in 2009 [15], we reported that the Ge-based technology promises a significantly improved NBTI robustness. To benefit from this property, the SiGe gate-stack was optimized for enhanced reliability, including a high Ge fraction (55%) in the channel, a sufficiently thick quantum well (6.5 nm) and a Si passivation layer of reduced thickness (0.8 nm) [16,17]. By means of such optimization, we demonstrated sufficiently reliable ultra-thin EOT SiGe pMOSFETs with a 10 year lifetime at operating conditions in both gate-first and gate-last process flows (Fig. 2) [18]. The main gate-stack parameter affecting the NBTI robustness was found to be the Si passivation layer thickness, with thinner Si caps consistently observed to yield a significant boost of the device reliability while

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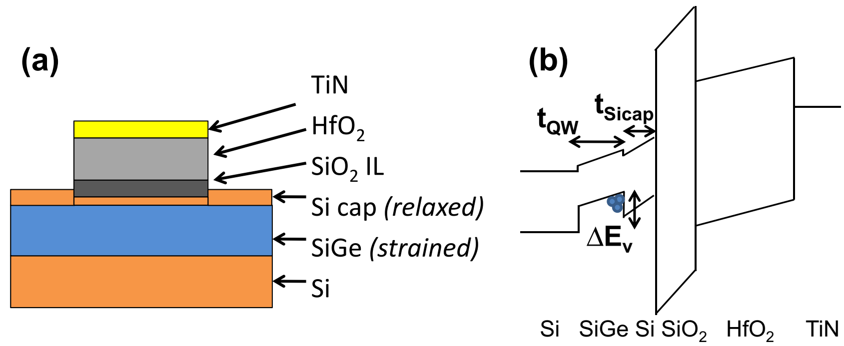

Fig. 1. (a) Sketch of the gate-stack of SiGe devices used in this work. (b) Band diagram in inversion. Channel holes are confined into the SiGe quantum well due to the valence band offset (ΔE_v) between the SiGe channel and the Si cap. The Si cap thickness (t_{Sicap}) therefore contributes to the capacitance equivalent thickness in inversion (T_{inv}) of the gate stack.

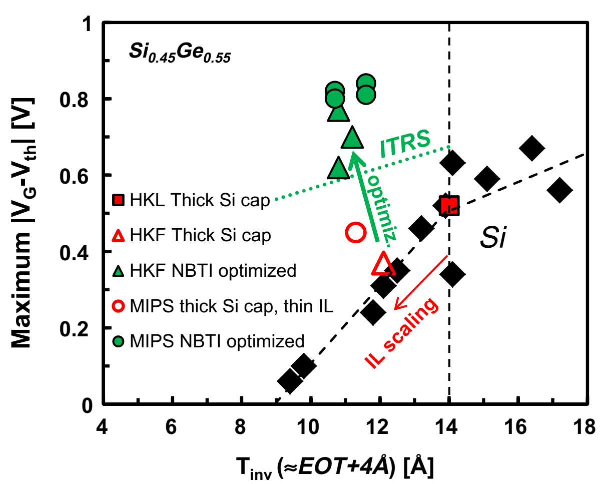

Fig. 2. A high Ge fraction (55%) in a 6.5 nm thick quantum well, combined with a thin Si cap (0.8 nm) boost the maximum operating overdrive ($|V_G - V_{th0}|$) to meet the target V_{DD} at ultra-thin EOT in a MIPS flow (solid circles, as compared to open circle). The optimization was also implemented in a RMG flow: high-k last SiGe sample with thick Si cap (solid square) shows poor NBTI robustness; an IL reduction by means of O-scavenging in a high-k first process flow (open triangle), further increases NBTI; however, the SiGe gate-stack optimization (solid triangles) boosts the maximum operating overdrive above the ITRS target. The results were reproduced for several process thermal budgets.

reducing the capacitance equivalent thickness in inversion (T_{inv}) of the gate stack (Fig. 3). Furthermore, the reliability improvement was observed to be readily transferable to different device structures such as pure Ge channel pMOSFETs and wrapped SiGe channel pfinFETs [19]. These process- and architecture-independent results suggest the superior reliability to be an intrinsic property of the MOS system consisting of a Ge-based channel and a SiO_2/HfO_2 dielectric stack. It is therefore eminently relevant to understand in detail the physical mechanisms behind this property.

By comparing with Si reference devices with an identical high-k/metal gate stack, we have reported several experimental observations about the NBTI degradation kinetic in optimized SiGe channel devices [19], which can be summarized as:

(1) Similar time dependence (i.e., the same power-law exponent) of the overall threshold voltage shift (ΔV_{th});
(2) Similar apparent temperature activation [12] of the overall ΔV_{th} ($E_A \approx 60$ mV);
(3) Reduced interface state generation (ΔN_{it}, the so-called *permanent* component of NBTI [20]) and significantly reduced hole trapping in pre-existing bulk oxide

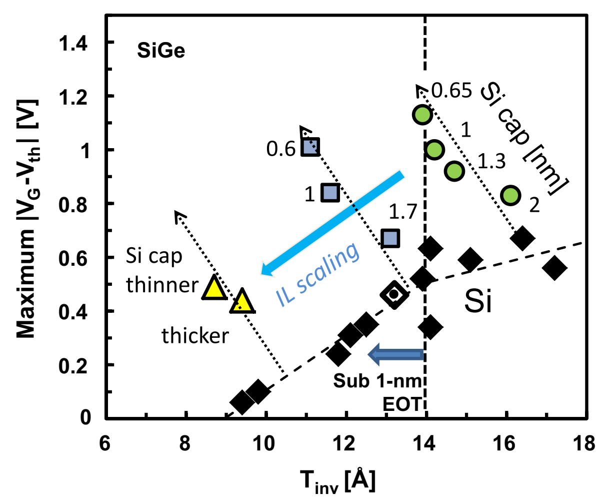

Fig. 3. Maximum operating overdrive for 10 year lifetime ($T = 125$ °C, failure criterion $\Delta V_{th} = 30$ mV) vs. T_{inv}. SiGe devices with a thin Si cap offer improved NBTI reliability, i.e. higher maximum operating overdrive.

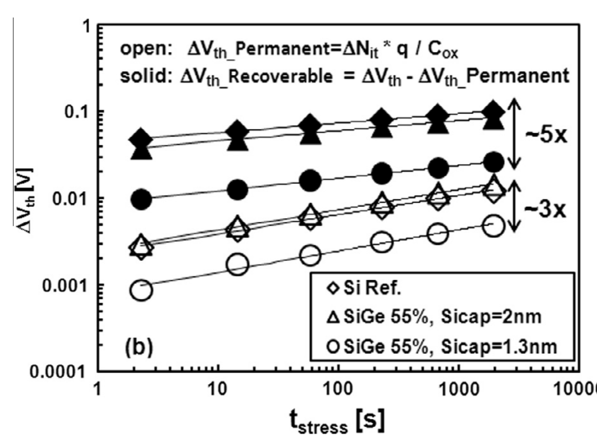

Fig. 4. Total ΔV_{th} split into the so-called permanent (*P*) ΔV_{th}, assumed to be caused by ΔN_{it}, and the recoverable (*R*) ΔV_{th}, assumed to be caused by filling of pre-existing oxide traps (N_{ot}). ΔN_{it} measured with charge pumping during NBTI stress were converted to $\Delta V_{th\_Permanent}$ ($=\Delta N_{it}.q/C_{ox}$) in order to decouple their contribution from the total measured ΔV_{th}. Three samples are compared (Si Reference, SiGe with thick and thin Si caps): ΔN_{it} follows a power law on the stress time with the same exponent (~0.25) on all the samples. However SiGe devices with thinner Si cap show both reduced *P* and *R*, with the reduction of *R* having a higher impact on the total ΔV_{th}.