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RTN assessment of traps in polysilicon cylindrical vertical FETs for NVM application

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ABSTRACT

In this work the drain current random telegraph noise (RTN) in polysilicon-channel cylindrical vertical FET structures is studied experimentally. We show that single electron trapping events can induce significant drain current fluctuations during read operation in deeply scaled non-volatile memories (NVMs). Low-frequency (LF) noise and capture and emission time constants of the traps are also analyzed at different gate and drain bias conditions. Two independent types of traps are identified in this study, which we categorize as slow and fast states. In this paper, we show that the RTN most likely originates from traps in the highly defective channel region, in addition to the fluctuations caused by defects in the oxide close to the interface with the channel.

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1. Introduction

The polysilicon cylindrical vertical FET devices are emerging as the most promising alternative for further downscaling of 10 nm NVMs (non-volatile memories) due to the following reasons. First, the cylindrical geometry of these devices with the gate all around boosts the program and erases performances. And second, the punch-and-plug architecture of these devices allows stacking vertically a high number of cells; therefore, scales the cost per bit and relaxes the physical feature size [1–4].

However, the device miniaturization, leading to a reduction of the number of carriers available for transport, gives rise to a great sensitivity to inevitable device variations. In other words, a few critical defects have a marked impact on the device operation. Random telegraph noise (RTN) consists of the temporal switching of the current or voltage between two (high and low level) or several states that is controlled by charging and discharging of a single defect. Important parameters of RTN are the time spent in the high current state corresponds to τ_c (capture time) and τ_e corresponding to the time spent in the low current state (emission time). Due to the technology scaling, it becomes a reliability issue and offers the opportunity of studying the trapping and detrapping behavior of single traps [5–9].

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Besides the traditional gate oxide traps as a source of RTN fluctuations, the polysilicon body presents many grain boundaries that enhance the percolated conduction between drain and source. It is expected that trapping and detrapping through oxide traps and poly-Si defects may equally induce RTN-fluctuations in the channel current. However, a different dependence on gate and drain bias can be expected for SiO_2 and poly-Si traps.

The aim of this work is to analyze experimentally the RTN of n-type polysilicon cylindrical vertical transistors to better understand the behaviour of gate oxide, interface and polysilicon traps.

2. Experimental

The polysilicon cylindrical vertical devices under investigation have a length (L) of 200 nm, a diameter of 45 nm, and the channel is practically undoped. The usual ONO stack of NVM memories was intentionally replaced by a 10 nm-SiO_2 layer in order to decouple the strong effect of the nitride trapping layer. The processing details can be found elsewhere [10].

Fig. 1 displays the polysilicon cylindrical vertical structure indicating the gate, source and drain, channel length (L) and its cross-section view of the channel region. Two measurement set-ups were used. For low-frequency and RTN noise measurement of the fast trap, we took advantage of the BTA hardware under control of ProPlusSolution software. For RTN (low trap), the source current I_S was registered as a function of time by means of a Keithley 2602A Source Measure Units (SMUs) for 600 s with a sampling

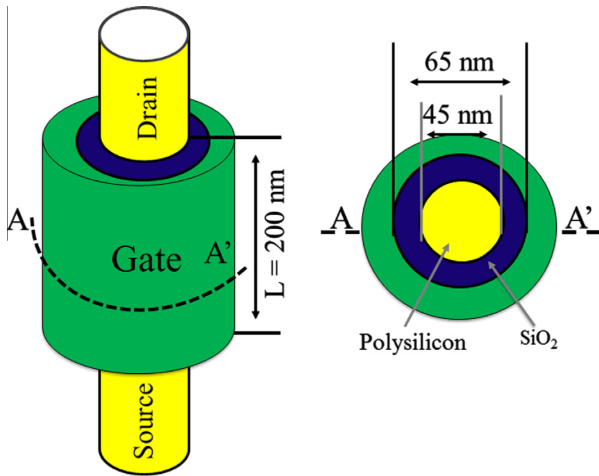


Fig. 1. Schematic view of a polysilicon cylindrical vertical FET device and its schematic representation of the cross-section along the channel (A A′).

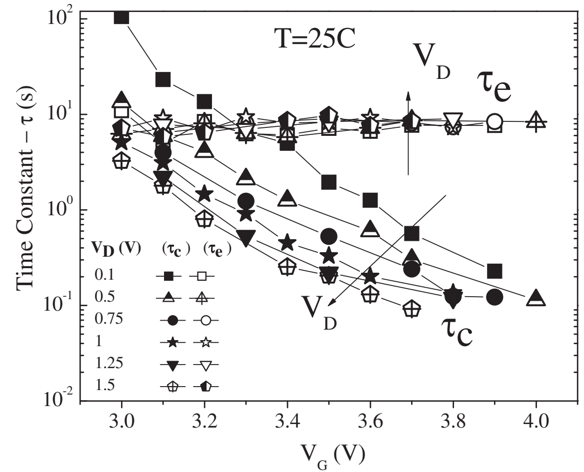


Fig. 4. The capture time constant (τ_c) and emission time constant (τ_e) as a function of the gate voltage (V_G) for different drain voltages (V_D) for the *slow trap*.

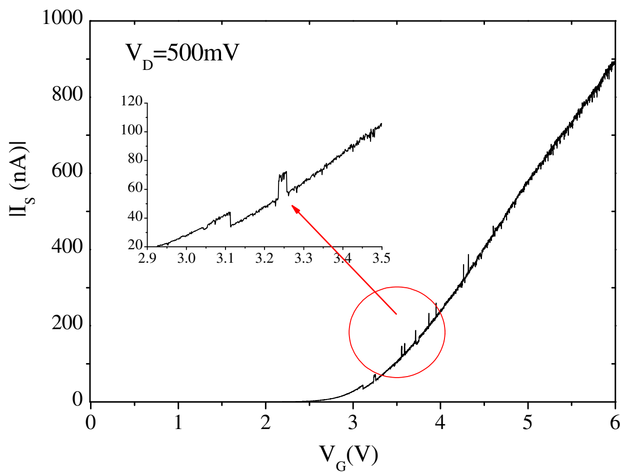
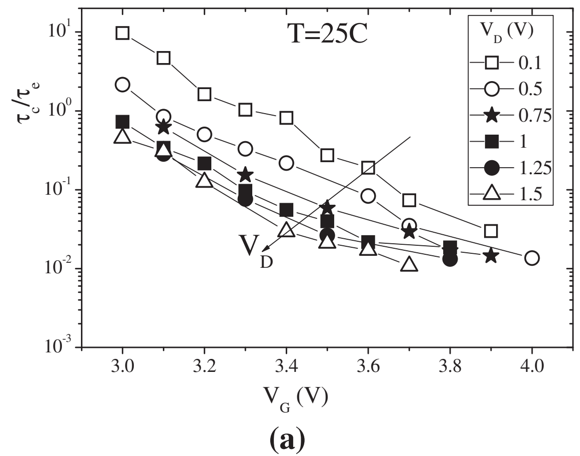


Fig. 2. Source current (I_S) as a function of the gate voltage (V_G) with 1 mV resolution and a V_D = 500 mV a for polysilicon cylindrical vertical device.



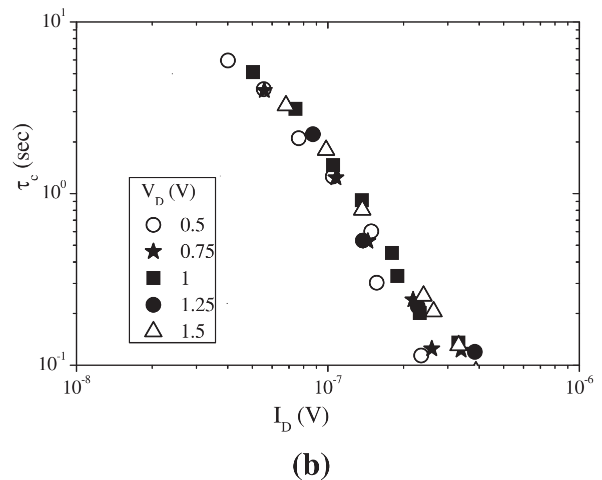


Fig. 5. (a) The calculated ratio τ_c/τ_e ratio as a function of the gate voltage (V_G) and (b) the capture time constant (τ_c) as a function the source current (I_s) of the *slow trap*.

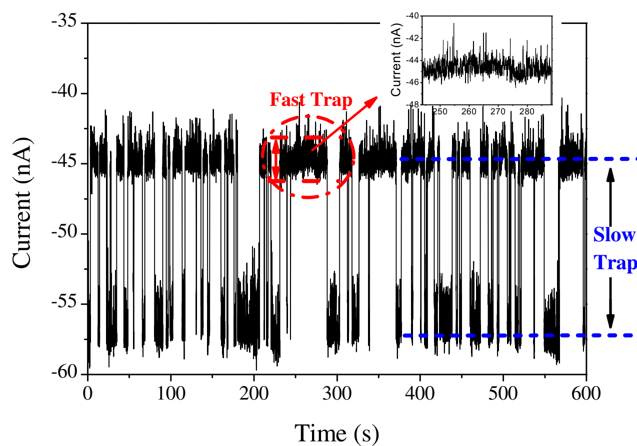


Fig. 3. RTN (IS) as a function of the time for V_G = 3.2 V and V_D = 500 mV showing trapping and detrapping of a fast and a *slow trap*.

time of 20 ms. The 1/*f* noise and RTN measurements were performed as a function of gate voltage in linear and saturation operation.

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