



Gate-last integration on planar FDSOI for low- V_{Tp} and low-EOT MOSFETs

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ABSTRACT

We integrated planar fully depleted (FD) SOI MOSFETs with a gate-last on high-k first (GL-HKF) down to gate lengths of $L_g = 15$ nm and active widths of $W = 80$ nm. Such an integration scheme enables reaching for pMOSFETs a threshold voltage of $V_{Tp} = -0.2$ V and one decade gate current (J_G) gain, as well as similar hole mobility and ON-currents, compared to pMOSFETs integrated with a gate first. This approach is also benchmarked with high-k last (GL-HKL) stacks in terms of leakage, equivalent oxide thickness (EOT), effective work-function (EWF) and flat band voltage (V_{FB}) shift under stress.

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1. Introduction

Contrarily to bulk, FDSOI devices require gate effective work-function (EWF) at only ≈ 250 mV from the silicon midgap to obtain low- V_{Ts} transistors. In order to reach this specification various techniques can be used and combined: additives such as Al or La can be added into the gate to lower the V_T of pMOSFETs or nMOSFETs respectively [1], V_{Tp} can be tuned by using SiGe channels [2]. In FDSOI technology, ground planes below the buried oxide and body bias capabilities offer an additional leverage [3]. Gate-last (GL) technology is another solution demonstrated with a high-k first (HKF) [4] or a high-k last (HKL) [5] on bulk substrates or even on SOI [6]. Furthermore, this integration allows to address equivalent oxide thickness (EOT) required for sub-20 nm technology node. In this study, we demonstrate that gate-last integration can be used on planar FDSOI to reach EOT below 1 nm and EWF values from midgap up to 5 eV.

2. High-k first gate-last pMOSFETs integration

FDSOI transistors with 7.5 nm ultra-thin body and 25 nm thin buried oxide with a HfSiON first and TiN last (2, 3, Fig. 1) have been fabricated as described in Fig. 2. Plasma oxidation is used for the interfacial layer formation, then the HfSiO is deposited and

nitrided following by a 950 °C post-deposition anneal. Then Si source/drain are epitaxially raised and the silicide is formed. The PMD is deposited and planarized before dummy poly-Si gates removal with TMAH. The final metal gate stack includes 10 nm of physical-vapor-deposited (PVD) TiN, two different TiN capping (MOCVD or ALD) and W. The use of this TiN ALD (Atomic-layer deposition with TDMAT precursor and N_2 remote plasma) as capping allows depositing thinner layers, thus making it more suitable to fill short gate lengths. The excess metal is polished off followed by contact processing (Fig. 2).

3. Results

The pMOS I_{ON} – I_{OFF} tradeoff (Fig. 3) of GL devices are similar to those of gate-first (GF) reference, when both are integrated without mechanical boosters. This is due to a similar EOT and hole mobility at high effective field (Fig. 4). Nevertheless, the NBTI of GL pMOSFETs is slightly degraded (Fig. 5). The gate stack with ALD capping (3), which presents a better performance and reliability than the MOCVD capping (Figs. 3–5), also yields the lowest V_T of -0.2 V (Fig. 6). The flat band voltage variation (ΔV_{FB}) has also been extracted with capacitance vs. voltage measurement considering the Silicon midgap as reference level [7]. This low- V_T is in agreement with the extracted high EWF ($\Delta V_{FB} = 0.35$ V). In order to better understand this result, we integrated MOS capacitors on bulk with a similar process flow than in Fig. 2 with different thicknesses of TiN PVD as gate metal and TiN ALD capping (3' Fig. 7). We found

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Ref.	Substrate	High-k	Dummy Si-poly	Metal Gate	Gate capping
1 GF	SOI	HfSiON 1.9nm 950°C	no	TiN PVD	Si-poly
2	SOI	HfSiON 1.9nm 950°C	yes	TiN PVD	5nm TiN MOCVD +W
2'	bulk	HfSiON 1.9nm 950°C	yes	TiN PVD	5nm TiN MOCVD +W
3	SOI	HfSiON 1.9nm 950°C	yes	TiN PVD	2.2nm TiN ALD +W
3'	bulk	HfSiON 1.9nm 950°C	yes	TiN PVD	2.2nm TiN ALD +W
4 GF	bulk	HfO ₂ +N 2nm 650°C	no	TiN/Al/TiN	Si-poly
5	bulk	HfO ₂ 2nm 500°C	no	TaN	5nm TiN ALD +W

Fig. 1. Summary of gate stacks configurations investigated in this work.

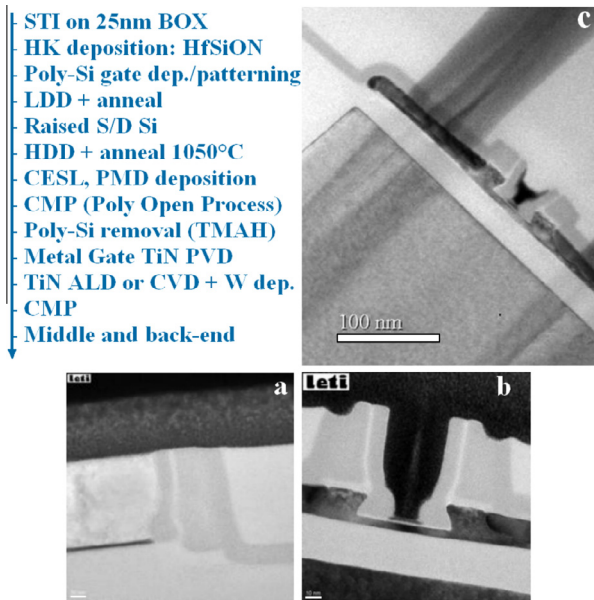


Fig. 2. Gate-last process flow and TEM pictures of a FDSOI pMOSFET: (a) after the POP CMP (b) after poly-Si removal (c) after back-end.

out that both TiN are highly P+ and that increasing the TiN thickness decreases the EWF. TiN ALD itself has an EWF above 5 eV and a 10 nm thick TiN PVD has an EWF of 4.9 eV as obtained in [8] with a TiN last on HfO₂ at the same EOT of 1.1 nm. Such high EWF values are known to be due to the creation of dipoles at the metal/dielectric interface [9]. On the other hand, the GL integration with a TiN MOCVD capping (2) is only 150 mV above midgap (Fig. 8). Compared to TiN ALD, the same TDMAT precursor is used but the impact of N₂/H₂ plasma may explain the EWF difference and the high-k degradation as evidenced by the mobility and NBTI data (Figs. 4 and 5). EWF of GF MOSFETs is 100 mV below the midgap (1) and the insertion of 0.22 nm Al in the gate stack yields a midgap gate (4, Fig. 8). Finally, the J_G -EOT relationship (Fig. 9) shows a leakage current four decades lower with our best stack with TiN PVD metal gate and TiN ALD capping (3) than with the

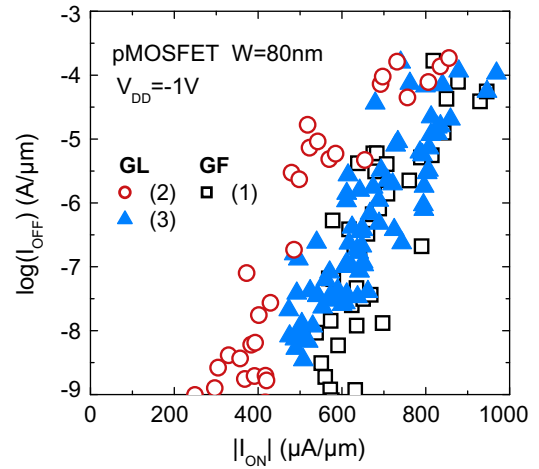


Fig. 3. I_{ON} - I_{OFF} trade-off of GF and GL pMOSFETs at $V_{DD} = -1$ V. $W = 80$ nm, $L_{g,nom} = 50$ nm.

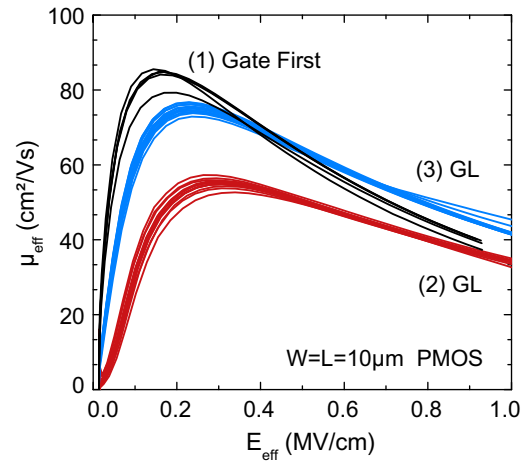


Fig. 4. Hole mobility vs. E_{eff} in long channel pMOSFETs ($L = 10$ μm).

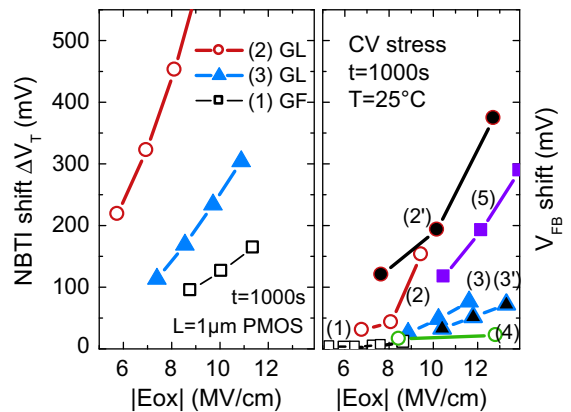


Fig. 5. NBTI measurements ($L_g = 1$ μm pMOSFETs) and V_{FB} shift with stress (pMOS capacitors) vs. oxide field.

same SiO₂ thickness. This corresponds to one decade J_G reduction compared to a GF integration (1). Note that pMOSFETs on SOI present a lower J_G than equivalent capacitors on bulk (2', 3') due to a limitation of the substrate current.

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