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Optimized electrode and interface for enhanced reliability of high-k based metal–insulator–metal capacitors

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ABSTRACT

This paper focuses on zirconia and TiN based MIM buffer capacitors integrated in immediate vicinity to the Si substrate. Process variations and integration schemes are investigated regarding their influence on capacitance, leakage current and reliability characteristics. Especially, the effect of interface pre-treatments between the Si substrate and the bottom electrode as well as processing conditions of the TiN top electrode is studied in detail.

It is shown that the reliability of high-k MIM capacitors is significantly dominated by the kind of pre-treatment of the Si substrate and also by the deposition temperature of the metal nitride top electrode. As a result, it is recommended to introduce chemical oxidation of the substrate before MIM deposition as well as lowering the deposition temperature to about 400 °C for the top TiN electrode in order to enhance the lifetime of the MIM dielectric.

1. Introduction

Progressive miniaturization of electronic devices such as of smartphones or sensors for medical, industrial and automotive applications requires smaller substrates and form factors. This drives amongst others the integration and scaling of space consuming external passive components on chip (SoC) or package (SiP) level. Consequently, there is a great interest to integrate capacitors with high-k dielectrics to achieve higher capacitance densities for buffering and decoupling purposes [1]. Intensive material tuning is necessary to meet the electrical requirements for these applications with respect to capacitance density, leakage and reliability. Additionally it is crucial to understand the interactions between substrate, electrodes and dielectric in order to optimize the properties of the widely-used metal–isolator–metal (MIM) capacitors [2]. This paper focuses on zirconia and TiN based MIM buffer capacitors integrated in immediate vicinity to the Si substrate. Process variations and integration schemes are investigated regarding their influence on capacitance, leakage current and reliability characteristics. Especially, the effect of interface pre-treatments between the Si substrate and the bottom electrode as well as processing conditions of the TiN top electrode is studied in detail.

2. Experiment

Planar MIM capacitors were fabricated on n- and p-doped 300 mm Si wafers using industrial grade wafer processing equipment. After different substrate pre-treatments (native oxide-natOX, HF-dip and wet chemical oxidation using SC1 – chemOX) 10 nm TiN bottom electrodes (BE) were deposited at 450 °C followed by 12–21 nm thin high-k ZrO_2–Al_2O_3–ZrO_2 (ZAZ) laminates at 275 °C, both prepared by atomic layer deposition (ALD). The TiN top electrodes (TE) of 50 nm were deposited by pulsed CVD at temperatures between 400 °C and 500 °C. The physical thicknesses of the dielectric films were determined by spectroscopic ellipsometry and transmission electron microscopy (TEM). In order to clarify the element distribution in the MIM film stacks and especially the capacitors top interface influenced by different TE deposition temperatures, time-of-flight secondary ion mass spectrometry (ToF-SIMS) measurements were applied in the dynamic mode.

Capacitor test chips were patterned by electron beam lithography and wet chemical etching of the top electrode. The MIM device wafers were characterized on automated probing stations regarding electrical performance (CV, IV) and time dependent dielectric breakdown behavior (TDDB) considering statistics of 36 chips.

3. Results and discussion

In Fig. 1 TEM micrographs show MIM capacitors with different interfaces to the Si-substrate. The comparison between a capacitor

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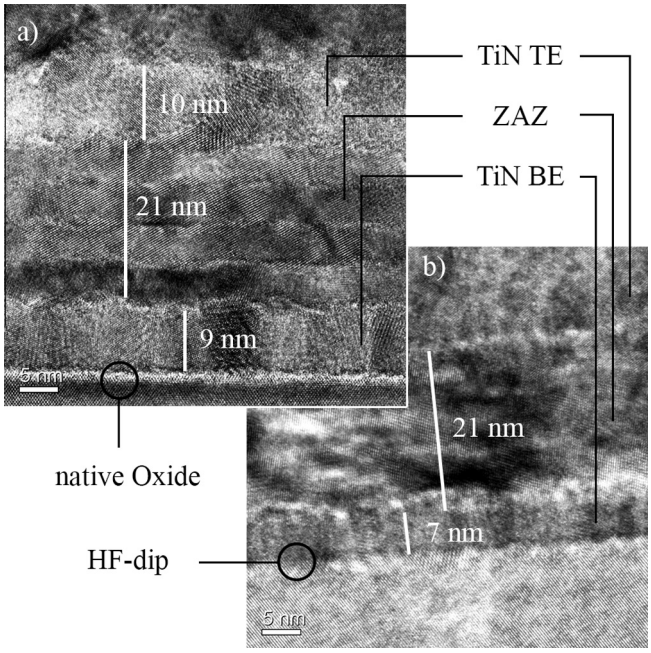

Fig. 1. TEM micrograph of MIM capacitors on (a) native oxide interface and (b) on HF dipped substrate.

on native oxide (Fig. 1a) and deposited on an HF dipped surface (Fig. 1b) confirms that HF dipping removes the interface oxide.

According to the capacitance behavior shown as sample set (a) in Fig. 2 different substrate pre-treatments before the bottom TiN electrode deposition seem to have no significant impact on the performance of MIM capacitors. Also the leakage current measurements reveal no difference between the I–V curves, and ToF-SIMS depth profiles provide the similar MIM stack composition for each pre-treatment (graphs not shown). Of course, a difference of the interface between BE and Si-substrate with less oxide after the HF-dipping could be detected in agreement with the TEM micrographs. However, considering breakdown voltages and TDDB characteristics (see sample set (a) in Figs. 3 and 4) a chemical oxidation of the Si-substrate improves the reliability performance significantly, independent of the kind of substrate doping. By interpolating the TDDB data with the conservative linear E-Model the capacitors with chemical oxide would meet 10 years life time up to electric fields of about 2.2 MV/cm based on 15 k μm^2 capacitor area.

As shown in Fig. 5, the deposition temperature of the TE has a substantial impact on the MIM leakage current characteristics. A lower TiN deposition temperature leads to a significant reduction of device leakage current while keeping the dielectric capacitance nearly constant (Fig. 2 sample set (b)).

This observation applies also for different dielectric film thicknesses. The slight capacitance increase for the higher TiN deposition temperature is supposed to be related to a decrease of the effective high-k thickness due to diffusion or "spiking" of TiN from the top electrode into the high-k dielectric layer. Another possibility could be a stronger densification of the high-k due to the higher temperature. The higher temperature budget seems to enhance the TiN diffusion along ZAZ grain boundaries causing early dielectric breakdown of the 12 nm thin ZAZ laminate with 450 °C TE deposition temperature (therefore not shown). The higher TE deposition temperature leads probably also to an increased defect density at the top interface which results in an asymmetric charge injection from the electrodes. As a consequence higher leakage currents, lower breakdown voltages and higher bias asymmetries are observed for negative polarity (Fig. 3b). These results are supported

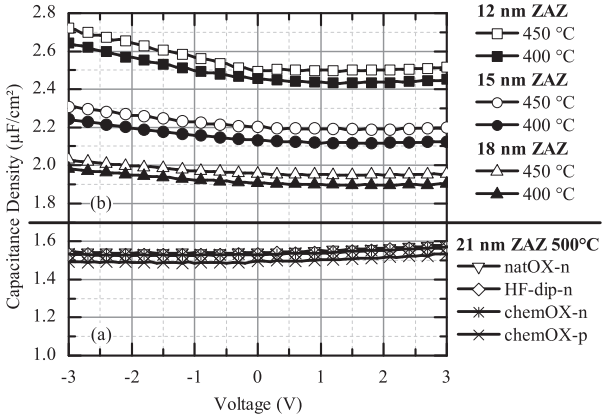

Fig. 2. C–V characteristics of (a) different substrate pre-treatments and (b) high-k thicknesses (12–18 nm) comparing 400 °C and 450 °C TE deposition temperatures.

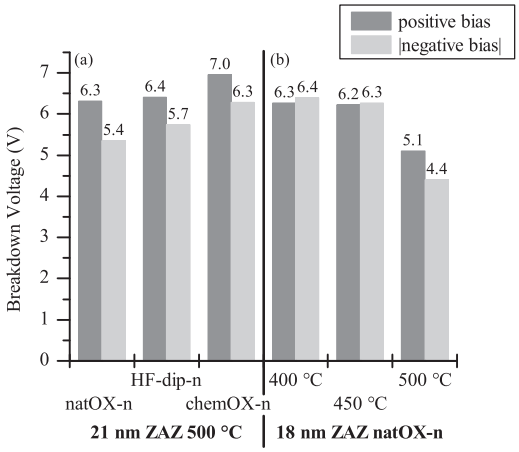

Fig. 3. Positive and negative breakdown voltages of MIM capacitors with (a) different substrate pre-treatments for 21 nm high-k thickness and with (b) a variation of the TE deposition temperature from 400 °C to 500 °C for 18 nm high-k layers.

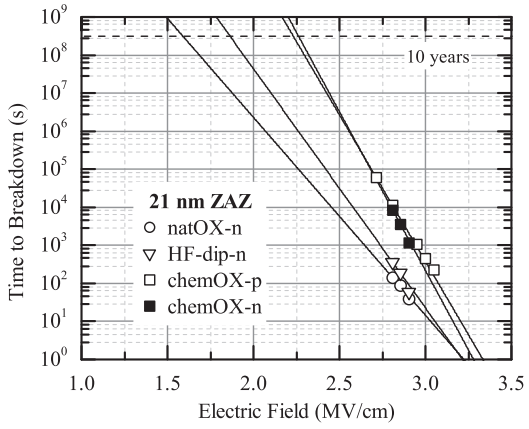

Fig. 4. Mean-time-to-dielectric-breakdown as a function of the electric field for 21 nm high-k MIM capacitors and different substrate pre-treatments.

by ToF-SIMS depth profiles of the MIM capacitors with 15 nm high-k thickness in Fig. 6. Most significant is the enlarged intermixing region at the top interface but also at the bottom interface which was already described in literature [2] for the sample with