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Exploration of multilayer field-coupled nanomagnetic circuits

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ABSTRACT

Unlike MOSFET technology, Field-Coupled Nanocomputing (FCN) structures are based upon a completely new computational paradigm. The basic computational element propagates the information through near-field interaction with neighboring elements. The potential of this principle is really promising because of the absence of current flow, leading to low power consumption. Here, we explore the in-plane NanoMagnetic Logic implementation. The analysis of complex circuits highlights the limitations due to their planar structure: mixing logic and interconnections on a single layer leads to an explosion of the circuit area. In this paper, we evaluate whether a 3D implementation of the structure can abruptly reduce the major limitation of the technology. We propose a solution by using a particular clock delivery method, named Virtual Clock. The analysis is carried out through micromagnetic and functional simulations on medium complexity architectures. The results obtained clearly highlight a large improvement in circuit area and power consumption.

1. Introduction

The International Technology Roadmap for Semiconductors (ITRS) [1] predicts that, in few years, MOSFET technology scaling will arrive at a point where it will not be possible to make further progress. There are three limitations that narrow further transistors scaling: 1) In deep-scaled devices tunnel and leakage currents increase causing the worsening of performance and power consumption. 2) Current lithography-based techniques are not able to provide the required resolution in order to fabricate nano-transistors; 3) Production, equipment and testing costs may become excessively high.

As a response to the impending end of the CMOS scaling, electronics is moving toward three-dimensional structures. Along with this trend, the scientific community is focusing its attention toward beyond-MOSFET technologies that allow, by their nature, to implement 3D circuits [2]. The aim of this paper is to make an innovative contribution by mixing these two tendencies. We propose structures that exploit the vertical dimension based on one of these emerging technologies, NanoMagnet Logic (NML) [3], in particular the in-plane implementation (iNML). NML is: 1) A low power technology (the dynamic power consumption is potentially low and there is no static consumption) [4]. 2) Immune to radiations. 3) Non-volatile because of its magnetic nature and, thus, it gives the possibility to embed logic and memory in the same device [5,6].

So far researchers have focused their work on planar iNML circuits, i.e. circuits that are placed on one physical layer [7]. However, the higher the complexity, the more interconnections impact on the circuit structure causing the area to explode [8]. This has also a significant effect on the growth of the circuit latency and on the power consumption [9]. The multi-layer design presented in this work effectively solves the problem of interconnections overhead, requiring that iNML circuits are distributed not on a single plane but on two or more different physical layers – implementing indeed three-dimensional structures.

In this paper, we show how the availability of other layers allows a great reduction of area occupation, latency and power consumption. We thoroughly demonstrate the potentialities of this approach, introduced in a preliminary form in Ref. [6], analyzing the problem at different abstraction levels, as described in section 3. The 3D concept is verified by means of micromagnetic simulations (Section 4). Different circuit layouts of both planar and multi-layer implementations are proposed and compared. Planar and multi-layer circuits are modeled in VHDL firstly. Then, functional simulations are performed to verify their correctness (Section 5). As a last step, performance of both implementations are compared and discussed in section 6. In addition, the preliminary results of the Full Adder and the 4-bit Ripple Carry Adder presented in Ref. [6] are compared with the perpendicular implementation of the NML. This demonstration, even though based on models and simulations and not on experiments, paves the way to a new direc-

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tion in the study of this technology (iNML) and of the Field-Coupling Nanocomputing principle in general.

2. Background

NanoMagnet Logic (NML) technology uses single domain magnets as basic cells [10]. In order to guarantee the presence of a single magnetic domain, magnets must be sufficiently small (few tens of nanometres). Nanomagnets are bi-stable cells. Thanks to properties such as shape or magneto-crystalline anisotropy, nanomagnets can have only two magnetization stable states used to map logic '0' and '1' (see Fig. 1A) [11]. Two families of NML circuits can be distinguished: in-plane NML (iNML) and perpendicular NML (pNML). In the first case, the magnetization vector lies in the magnet plane [12], while in the latter case the magnetization is perpendicular to the magnet plane [13,14].

Multilayer circuits in pNML technology were already theorized and fabricated [2,15,16]. In this work, we focus on iNML, discussing and analyzing the possibility of developing multilayer circuits in this technology. Multilayer iNML structures have not been fabricated yet. Nevertheless, iNML and pNML are similar technologies, hence, this proves, in general, the feasibility of fabricating 3D NML circuits.

The reasons why we present an analysis of planar and 3D structures based on in-plane NML are manifold: first of all, iNML is much faster than pNML; in addition, differently from perpendicular NML, iNML is compatible with some interesting structures, such as domain walls, and with different types of clock mechanisms. Moreover, there exists the possibility of creating hybrid structures mixing iNML and pNML technologies that further justifies the exploration of iNML-based structures. Last but not least, this is the first work, to the best of our knowledge, that uses iNML to implement multilayer circuits. In section 5, a comparison between the two technologies is given. In any NML implementation, circuits are built aligning magnets on a plane. Information is driven by the magnetodynamic interaction among neighbouring cells which are coupled in an anti-ferromagnetic way. Fig. 1B depicts an inverter that, employing the anti-ferromagnetic coupling, can be simply implemented by linking an even number of magnets. The cross wire (Fig. 1C) is a structure that allows two wires to cross each other without interference. iNML is a majority-based technology meaning that its basic gate is the majority voter [17]. Its magnetic implementation is shown in Fig. 1D. The majority voter satisfies the logic equation $M(A,B,C) = AB + BC + AC$. It can also be used as a logic AND/OR fixing one of the inputs to 0/1 [18]. These blocks constitute a complete logic set and allow to built any logic circuit. As we demonstrated in Ref. [19], a structure that can be used as interconnection in iNML circuits is the domain wall (Fig. 1E) [20]. Domain walls embedded in iNML circuits are forced in reset state by a magnetic field, similarly to nanomagnets. When the magnetic field is removed, a domain wall is nucleated inside the magnetic stripe, propagating the information at long distances. The magnet at the end side of the domain wall will reach a new state depending on the value of the domain wall. Domain wall interconnections are far more efficient than nanomagnets interconnections [19,21].

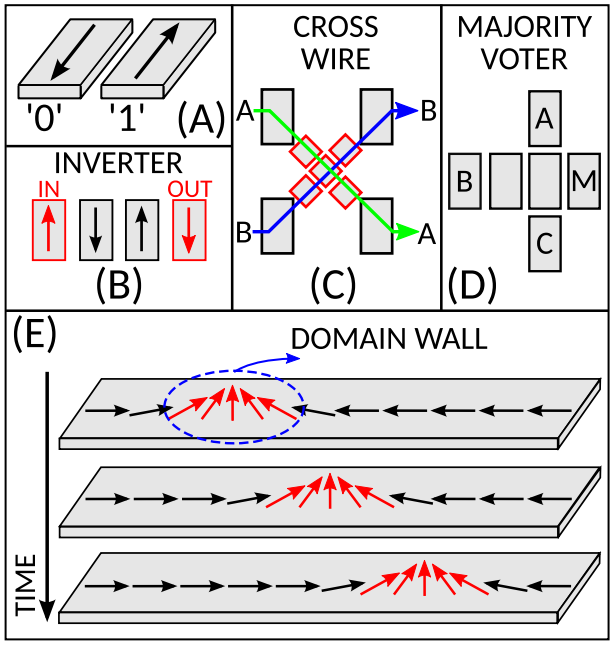

Fig. 1. (A) iNML stable magnetization states and correspondent bit coding. (B) An iNML wire that works as inverter. (C) Cross wire. (D) Majority Voter (MV). (E) Domain wall.

2.1. Need for clocking

As mentioned before, information propagation depends on the magnetodynamic interaction among neighbouring cells: when a nanomagnet switches in a stable state, the adjacent cells switch accordingly. However, the magnetic field generated by one magnet is not high enough to stimulate the switching of neighbouring cells, hence, an external mechanism, called clock, is required to help magnets switching. In the most classic implementation this external mean is a magnetic field that drives magnets in an unstable state, called reset, before stabilizing [22]. As shown in Fig. 2A, when the magnetic field is applied, cells are forced in reset, except for the first magnet that works as input. Once the clock is released, nanomagnets start switching one at a time propagating the input signal. Chains of magnets act as wires, thus they can be used to connect gates to implement complex circuits. The magnetic field is normally generated by a current flowing through a wire located under the magnets plane [22]. However, in long magnet chains, the propagation may be affected by errors because of the influence of external factors like thermal noise [23]. To avoid this, iNML wires are divided in small zones (containing maximum five chained magnets), called clock zones. Each clock zone is driven by a different clock signal. When using this system, to ensure a correct information propagation, clock signals must be out of phase implementing a multiphase clock scheme.

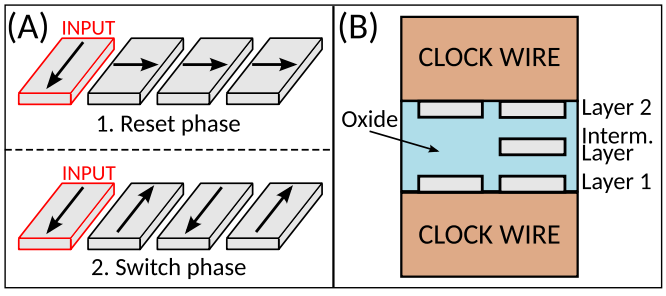

Fig. 2. (A) Clock mechanism: at first, magnets are forced in reset state (except for the input) by an external magnetic field that, once released, enables the anti-ferromagnetic switching of magnets according to the input element. (B) Multilayer structure composed of three layers: logic gates and interconnections are placed on layer 1 and 2 which are connected, vertically, through the intermediate layer.