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Integrated circuit for real-time poly-phase power quality monitoring

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ABSTRACT

Low power quality may cause serious problems in electricity networks, among them there are: reduction of equipment lifetime; false activation of protection devices; and increase in electrical and thermal losses. Considering this, it is very important to monitor electrical power quality of an industrial facility. This paper describes the architecture of an application-specific integrated circuit IP-core for power quality measurements. The main focus are the digital signal processing modules, which are designed based on IEC standards. The proposed Integrated Circuit, which uses TowerJazz 180 nm CMOS technology, comprises seven measurement channels for poly-phase systems and generates high precision estimation for power quality parameters. Experimental and simulated results are used to validate the proposed system.

1. Introduction

Electrical equipment performance may be directly affected by low power quality (PQ). In some cases, PQ disturbances produce serious problems that are often related to economical looses for utilities, suppliers and final consumers [1–3]. Considering this, ensuring the power quality is a main concern for proper electrical systems operation.

The International Electrotechnical Commission (IEC) is an important regulator for electrical power networks and within the IEC 61000 series of standards [4], most of the worldwide accepted boundaries for PQ indicators are defined, along with the adequate procedures to estimate such parameters.

Early identification of a potential problem should reduce the economical losses and also allow greater competitiveness for consumers and suppliers [5–7]. In some cases, industries may be severely economically affected whenever a PQ disturbance occurs. Considering this, the use of dedicated real-time PQ meters is increasing. Such equipment is able to perform detection, identification and recording of different PQ disturbances [8–10]. Real-time energy meters have been used, for example, in detection and classification of power quality disturbances [11–13], and for the control of photo-voltaic energy systems [14]. PQ information can also be used to activate disturbance mitigating strategies, or to turn off sensible loads whenever a serious problem occurs [15].

There are some dedicated PQ meters commercially available. The Texas Instruments MSP430F47197 comprises a general-use microprocessor and seven 10-bit analog-to-digital converters (ADC) [16]. It measures parameters of poly-phase systems such as root mean-square (RMS) value, instantaneous frequency and power. However, it does not comply with IEC standards. The ADE78801, from Analog Devices, also presents seven ADCs and is compliant with seven different standards including the IEC 61000-4-7 [17]. The Atmel 90E36A [18] is another commercial IC which uses seven 16-bit ADCs and the DSP modules are implemented in hardware. Unfortunately, as far as we know, none of these meters is compliant simultaneously with IEC 61000-4-30, 61000-4-7, and 61000-4-15 class-A standards.

Dedicated electronic measurement and signal processing devices have been also proposed recently for different applications such as triple-chamber pacemakers [19], medical equipment radiation detection systems [20], pulse oximeter systems [21], olive oil acidity determination [22], and electrochemical sensors [23].

This work presents the architecture of an Application-Specific Integrated Circuit (ASIC) intellectual property (IP) core designed to perform high accurate PQ measurements. The use of a dedicated integrated circuit based implementation allows production of fast and accurate results on a reduced unitary cost. The main focus of this work is the design and validation of the digital signal processing modules. Several parameters can be estimated with the proposed ASIC such as the instantaneous root-mean-square (RMS) values for voltages and currents, the

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harmonic distortion, and the active and apparent power. One of the major contributions of the proposed design is that all parameters are estimated in accordance to the IEC 61000 standards.

This document is organized as follows: in section 2 the main concepts and standards related to power quality are briefly described. The proposed system architecture is presented in section 3. A comparison between the proposed ASIC and other existing dedicated electronic solutions for power quality measurements is presented in section 4. The obtained experimental results are detailed in section 5. The conclusions are derived in section 6.

2. Power quality problems and standards

2.1. Most frequent power quality problems

In industrial electricity networks there is a large number of devices sensitive to PQ disturbances. In these cases, the presence of non-sinusoidal or non-standardized sinusoidal voltages or currents may generate problems such as over-heating, malfunctioning, premature aging and, in extreme cases, equipment failure [24]. Poor PQ also produces problems and additional losses in network components such as transformers and cables.

Considering that PQ is an essential aspect for electric power networks, there are several standards focused on the definition of measurement methods and acceptable ranges for some PQ parameters. Among them there is the IEC 61000-4 series of standards, which will be briefly described in the following.

2.2. IEC 61000-4-30 standard

The IEC 61000-4-30 [25] defines appropriated methods and minimum accuracy for measurement of different electrical parameters. Class A measurement methods are usually employed when precise results are required.

The fundamental frequency (f_0) estimation can be obtained using a 10 s time-window, in which the number of cycles is divided by the cumulative time-interval. Considering that harmonic and interharmonic components have been previously removed using a pre-processing filter (to avoid multiple zero-crossings), Equation (1) presents a method to estimate f_0 instantaneous value (within a given time-window) in a digital circuit using a clock-counter and zero-crossing identification:

$$f_0 = \frac{N_{\text{cross}}}{2 \cdot N_{\text{clk}} \cdot T_{\text{clk}}}, \tag{1}$$

where N_{cross} is the number of times the voltage signal crosses the zero-amplitude axis, N_{clk} is the number of clock cycles within the considered time-window and T_{clk} is the clock-cycle period.

The root mean square (X_{RMS}) value of the voltage (or current) can be computed over 10 or 12-cycles time intervals. An important voltage waveform quality parameter is the crest factor, which may be defined as in Equation (2):

$$C = \frac{|X|_{\text{peak}}}{X_{\text{RMS}}}, \tag{2}$$

where $|X|_{\text{peak}}$ is the absolute peak value of X. For perfect sinusoidal signals, $C = \sqrt{2}$, a different value indicates some kind of waveform distortion.

The RMS voltage value updated every half cycle is used to identify voltage oscillations by comparing with predetermined thresholds. A voltage dip (or swell) occurs when the RMS value stays under (or over) a given reference voltage value. An interruption is defined as the event in which the RMS value decreases under a voltage interruption threshold. For proper system monitoring it is important to identify the channel, the moment and the duration of a voltage oscillation fault.

The voltage unbalance factor between phases a, b and c (VUF) may be approximated using Equation (3):

$$\text{VUF} = \frac{82\sqrt{V_{abe}^2 + V_{bce}^2 + V_{cae}^2}}{V_{\text{AVG}}}, \tag{3}$$

where $V_{ije} = V_{ij} - V_{\text{AVG}}$ $(i = a,b,c;\ j = a,b,c;\ i \neq j)$, and V_{AVG} is the average line voltage.

2.3. IEC 61000-4-7 standard

The IEC 61000-4-7 standard defines procedures to estimate electrical systems non-linear distortion [26]. Non-linear loads introduce non-sinusoidal voltages (or currents) which produce harmonic and interharmonics components.

An estimation of the h-th order harmonic amplitude ($A_g(h)$) may be found by summing frequency-domain components (estimated through the discrete Fourier transform - DFT) adjacent to the harmonic frequencies. Considering that the h-th order harmonic component is $f_h = hf_0$, and using an interval equal to Δf, frequencies in the range $hf_0 - \Delta f/2 < f < hf_0 + \Delta f/2$ are considered. In this work, Equation (4) was used for harmonic amplitude estimation:

$$A_g(h) = \sqrt{\sum_{k=-\Delta f/2}^{\Delta f/2} [Y(hf_0 + k)]^2}, \tag{4}$$

where $Y(f)$ is the amplitude of the DFT for frequency f. This measurement is executed within a time interval of 10 or 12 cycles, for $f_0 = 50$ Hz or $f_0 = 60$ Hz power systems, respectively. Interharmonics are found similarly by summing the DFT amplitudes between the harmonic components.

The total harmonic distortion (THD) can be defined using Equation (5):

$$\text{THD} = \sqrt{\sum_{h=2}^{H} \left(\frac{A_g(h)}{A_g(1)} \right)^2}. \tag{5}$$

2.4. IEC 61000-4-15 standard

The IEC 61000-4-15 standard [27] deals with functional and design specifications for flicker measuring apparatus. The main purpose is to enable the construction of instruments to provide accurate flicker perception level for most practical voltage fluctuation waveforms.

Flickering was initially associated to the variation of light intensity in electrical lamps. The IEC 61000-4-15 adopts this effect as reference for flickering level estimation. It also defines estimation procedure and validation tests for the flickermeter, considering different frequency, amplitude and modulation scenarios.

3. Proposed system architecture

The proposed power quality measurement application-specific integrated circuit (see PQM-ASIC in Fig. 1) was designed to perform acquisition and digital signal processing of voltage and current information in poly-phase systems in order to estimate PQ indicators such as: root mean square (RMS) values; instantaneous frequency; crest factor; unbalance; harmonic distortion and power factor. For this, the proposed system must be connected to the analog instrumentation through an analog signal conditioning circuit. The designed ASIC comprises seven 16-bit analog to digital converters (ADCs). The ADC sampling frequency (f_S) is variable according to the line voltage fundamental frequency (f_0): $f_S = 15,360$ Hz for $f_0 = 60$ HZ and $f_S = 12,800$ Hz for $f_0 = 50$ HZ. For both cases $f_S = 256 f_0$, this choice allows to properly sample high-order harmonic components ($h \sim 100$).