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Design of low power comparator-reduced hybrid ADC

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ABSTRACT

This paper presents a new low-power comparator-reduced hybrid ADC. The proposed ADC uses dynamic comparators to perform a high-speed low-power conversion. In order to reduce the offset and kickback noise effect of conventional dynamic comparators, a new low-kickback noise comparator with a high pre-amplifier gain is presented. Two 4bit and 8bit ADCs are designed and simulated in 0.18 μm CMOS technology with 1.8 v supply voltage. INL and DNL of 4bit ADC are less than 0.4*LSB* and 0.5*LSB*, respectively, while 8bit ADC obtains DNL and INL of 0.83*LSB* and 1.3*LSB*, respectively. With ENOB of 3.6*bit* and 7.2*bit* for 4bit and 8bit ADCs, the 4bit ADC consumes only 1.7 mW at the sampling rate of 400 Ms/s and the 8bit ADC consumes 4.6 mW at the 80 MS/s.

1. Introduction

Low-resolution (4–6 bit) high-speed (>500 Ms/s sampling rate) ADCs play an important role in design of battery-powered systems based on standards like ultra-wideband (UWB) and wireless personal area networks (WPANs) [1,2]. Conventionally, the flash topology is used for high-speed low-resolution applications, due to the low-latency and high data-rate allowed by the topology [3]. However, conversion of flash ADCs in a single clock cycle is at the cost of an exponential dependence of area and power on the resolution [2]. Folding and interpolation techniques could be more suitable for low-power operation by reducing number of the comparators [2–4]. Beside, a pipeline ADC can break this exponential dependency [5,6]. In comparison with the flash ADC, the pipeline ADC uses fewer comparators at the expense of higher latency. Nevertheless, the linearity of pipeline ADCs is limited by finite open loop gain of residue amplifiers which consume considerable power at the high-speed operations [7]. A successive approximation register (SAR) ADC is an appropriate choice for low power applications since it utilizes only one comparator to complete a full conversion [8,9]. However, an N-bit SAR ADC needs N clock cycles to do a conversion which limits its usage for the high-speed applications.

The most of effective approaches such as folding and interpolating focus on reduction of comparators counts, since the comparators are the most power consuming part of flash topology. Besides, built-in offset voltage [10] and inverter [11] based comparators have been introduced to eliminate the resistive ladder which is second power consuming part of flash ADCs. However, Reduction of power consumption by omitting resistive ladder provides more non-linearity issues. This paper presents a comparator reduced hybrid ADC which uses analog switches in order to provide the proper reference voltage of each comparator. Dynamic comparators are used instead of conventional static comparators to obtain lower power consumption. Since dynamic comparators make decision at the rising or falling edge of clock signal, a timing sequence is designed to maximize the ADC throughput. A high-speed low-offset comparator with a low sensitivity to kickback noise effect is introduced to increase the ADC linearity. The rest of the paper is as follows. Structure of the proposed ADC and timing sequence of the comparators is described in section 2. Section 3 explains comparator design. Derivation of delay and pre-amplifier gain is provided in section 3, too. Reference voltage design is brought in section 4. Non-ideal effects are discussed in section 5. Section 6 shows simulation results and section 7 concludes the paper.

2. The proposed ADC design

A high-speed flash ADC needs $2^N - 1$ comparators for an N-bits conversion. Folding technique reduces the number of comparator by dividing the ADC to coarse and fine parts. The folding operation is normally performed using an amplifier which consumes lots of static power especially for high-speed and large folding factor. Interpolation technique reduces the number of pre-amplifiers, and thus reduces input capacitance. However, number of latches is same as flash topology. Changing reference voltages of comparators depending on input voltage can be used in order to reduce number of comparators, shown in

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Fig. 1. In this structure, N-bit conversion needs only N comparators. As illustrated for a four bit ADC, the reference voltage of each comparator changes regarding to output of the higher priority comparator. In order to have an appropriate design, the output level of comparators are change to −1 and 1 instead of 0 and 1. As en example, if input voltage would be $\frac{11V_{ref}}{32}$, the output of comparator of *comp*3 would be −1 since the negative input voltage of *comp*3 is $\frac{V_{ref}}{2}$. Regarding to output of *comp*3, negative input of *comp*2 changes to $\frac{V_{ref}}{2}-\frac{V_{ref}}{4}=\frac{V_{ref}}{4}$. As a result, the output of *comp*2 changes to 1. Negative input of *comp*1 changes to $\frac{3V_{ref}}{8}$ which provides −1 at the output of *comp*1. The same procedure determines the output of *comp*0, as illustrated in Fig. 1.

In fact, this technique introduces an appropriate trade-off between speed and power consumption. In comparison with typical flash topology this structure consumes less power. However, it is slower because of sequential behavior of comparators outputs. In other words, operation of this structure is same as a SAR ADC. Nevertheless, while a SAR ADC performs a conversion using a comparator along with the digital part and a N-bit Digital to Analog Converter (DAC), this structure uses N comparators for N bits conversion with the advantage of higher speed. Since the digital part of an SAR ADC consumes a significant power in high-speed applications, power consumption of this structure would be comparable with SAR ADCs as this structure does not need the digital part.

In order to perform a full conversion, each comparator should update its output as soon as its inputs change. As a result, this topology needs the static comparators to work properly. However, static comparators consume lots of power which is in contrast to idea of this topology, reduction of power consumption of conventional flash ADCs. The modified structure of Fig. 2 is proposed to reduce the power consumption of Fig. 1 topology using dynamic comparators. Dynamic comparators perform a comparison in two phases; pre-charge phase and evaluation phase. Dynamic comparators are prepared for comparison during pre-charge phase and then, comparison starts in evaluation phase. Consequently, the inputs of dynamic comparators should be ready before the evaluation phase starts. So the evaluation phase of inferior comparators (e.g. *comp0* and *comp1*) must starts after evaluation phase of superior comparators (e.g. *comp3* and *comp2*).

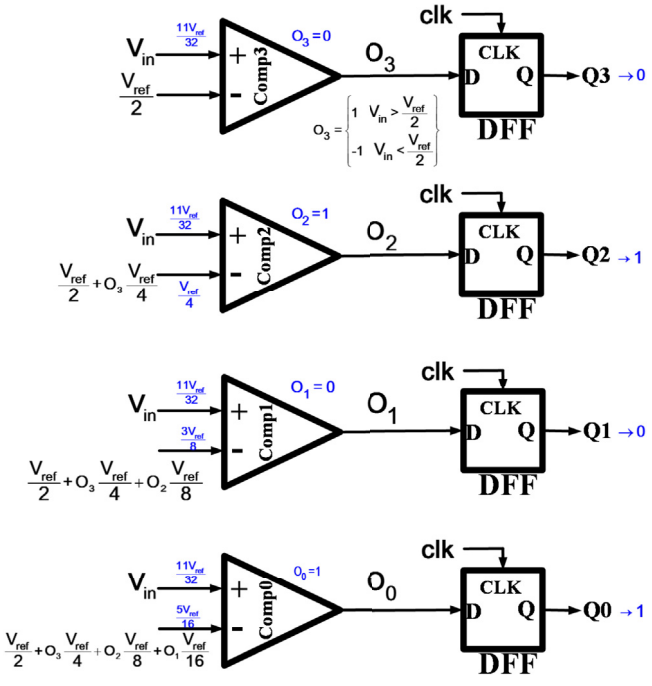

Fig. 1. Structure of comparator reduced hybrid ADC.

A clock generation chain is used to guarantee that evaluation phase of each comparator starts after preparation of comparator inputs. The comparators are in pre-charge phase when clock input is high and turn to evaluation phase when clock signal goes low. Since the pre-charge phase needs lower time in comparison with the evaluation phase, a variable pulse generator is used to reduce the pre-charge time and increase the evaluation time. An *XNOR* gate is used to determine completion of comparators comparison and then, an *OR* gate determines the evaluation time of following comparator. Timing waveform of clock signals is illustrated in Fig. 2b. When *clk1* is high, comparator of *comp3* is in pre-charge phase. *Comp3* goes to evaluation phase as soon as *clk1* falls to low level. All other comparators are in the pre-charge phase at this time. The output of *XNOR1* changes to low when the comparison of *comp3* completes. As a result, output of *OR1* falls down and the evaluation phase of *comp2* starts. This procedure is repeated for *comp1* and *comp0*. Although the proposed structure reduces the power consumption of conventional flash ADCs, it reduces the ADC conversion rate. Neglecting delay of voltage reference generators, the ADCs sampling rate for *N* bit conversion is limited by

$$f_{ADC_{\max}} < \frac{1}{N\tau_{comp}} \tag{1}$$

Where $f_{ADC_{\max}}$ is the maximum sampling rate of the proposed ADC and τ_{comp} is propagation delay of dynamic comparators.

3. Comparator design

Dynamic comparators have been developed in order to reduce power consumption and increase comparison speed of conventional static comparators [13]. Dynamic comparators use a low offset pre-amplifier to provide a signal level which is detectable by a following latch. The most popular latch consisting of two cross coupled inverters makes a strong positive feedback for a fast decision. Since the speed of the ADC is limited by the comparators delay, a high-speed low power comparator is a key building block of the proposed ADC.

A double tail voltage comparator shown in Fig. 3a was developed to increase the speed of conventional single tail dynamic comparators [14]. The comparator is in pre-charge phase when *clk* signal is high. As illustrated in Fig. 3b, the output of the pre-amplifier (*o*+ and *o*−) discharges to zero and both outputs of the latch (*out*+ and *out*-) charges to *Vdd* during pre-charge phase. The pre-amplifiers outputs start to charge regarding to input signals as soon as *clk* signal goes down (evaluation phase). In evaluation phase, the latch goes to regeneration state regarding to pre-amplifier outputs. As a result, one of the latch outputs falls to low depending on the input signals, demonstrating in Fig. 3b. Higher gain of pre-amplifier reduces both propagation delay and input-refereed offset voltage of the latch. However, propagation delay of the pre-amplifier is reduced by increasing pre-amplifier gain. In order to get a deeper understanding, gain of pre-amplifier and propagation delay of the comparator is calculated as follows.

Operation of the comparator in evaluation phase could be divided in two parts. The first part is between starting evaluation phase until the starting point of the regenerative latch. The starting point of the regenerative latch could be consider a time one of the output nodes discharges equals to a PMOS threshold voltage. The second part of evaluation phase is between starting the regenerative latch until the outputs become ready. We call the first part of latch as the *amplification phase* and the second part as the *decision phase*. Gain of the pre-amplifier during amplification phase for the small input differences could be written

$$A_{V_{pre-amp}} = \frac{g_{m2}}{C_o} t_{amp} \tag{2}$$

where, g_{m2} is trans-conductance of M2 or M3 transistors, C_o is total capacitance at the nodes of C_{o-} or C_{o+}, and t_{amp} is time of amplification phase which is the time between starting evaluation phase until one of