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High performance CMOS level up shifter with full–scale 1.2 V output voltage

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ABSTRACT

This paper introduces a very low static current CMOS level up shifter for low voltage single supply and high performance. The proposed low to high voltage level shifter is implemented using low threshold voltage transistors in 65 nm CMOS technology and based on differential topology. The shifter circuit was designed to be functional for an input voltage from 0.45 up to 1.2 V. Driving a 450 fF of capacitive load, the shifter's energy–delay product (EPD) is a 54% lower than a similar single supply level up shifter. Post–layout simulations, for every technological corner, temperature range from 25 up to 125 °C, operating input voltages and output capacitive loads (maximum of 740 fF), demonstrate the topology is fully functional without any impact on the static power consumption and the operating frequency of 500 MHz. Monte Carlo analysis shows the robustness of the proposed shifter within a 3σ device mismatch.

1. Introduction

The ever–growing demand of system–on–a–chip (SoC) devices in various sectors such as automotive and medical forces the use of efficient power management designs and nanometer CMOS technologies. A SoC operates with combined low–voltage and high–voltage supply rails using level–shifters as interface between these different power–supply domains. This requires design of level shifters that are optimized for reducing power consumption and delays in the critical paths. In Ref. [1] is presented a floating–voltage level shifter which shifts signal levels from circuit domain working with low–voltage power rails to circuit domain with floating power and ground rails. It offers a good rail slewing immunity. In Ref. [2], a subthreshold shifter uses a self–controlled current limiter to detect the output error for a robust voltage conversion. The design handles an input signal from 0.1 to 1.2 V. A level shifter to convert the lower logic levels into the higher ones is proposed in Ref. [3]. Bootstrapping techniques are employed to convert from the subthreshold supply to nominal supply in Ref. [4]. Other published solutions are based on a level–shifting capacitor [5] which is charged to supply a higher voltage at the input of the higher supply voltage stage achieving ultra–low power, short propagation delay, wide range of conversion voltage and high operation frequency.

In this work, a level up shifter with full–scale 1.2 V output voltage is designed with low–threshold voltage transistors and successfully verified in a 65 nm CMOS process. With differential technique, the proposed circuit operates with very reduced static current and low impacts from process and temperature variations. The circuit presented in this work achieves a fast and energy efficient voltage level conversion that works over a wide range of voltages. Simulation results at the high frequency of 500 MHz demonstrate that the proposed converter has a better energy–delay–product (EPD) performance than the previous art [2–6].

This paper is organized as follows: Section 2 presents the description of the proposed voltage level up shifter. In Section 3, post–layout simulation results and reliability analysis is provided. Section 4 compares the performance of the proposed converter against state–of–the–art designs. Finally, this brief is concluded in Section 5.

2. The level up shifter circuit topology

The topology showed in Fig. 1, *SC1*, provides differential input signals and uses a modified Differential Cascode Voltage Switch stage and an inverting output buffer [6]. This circuit achieves fast and energy–efficient voltage level up shifting and is based on self–adapting

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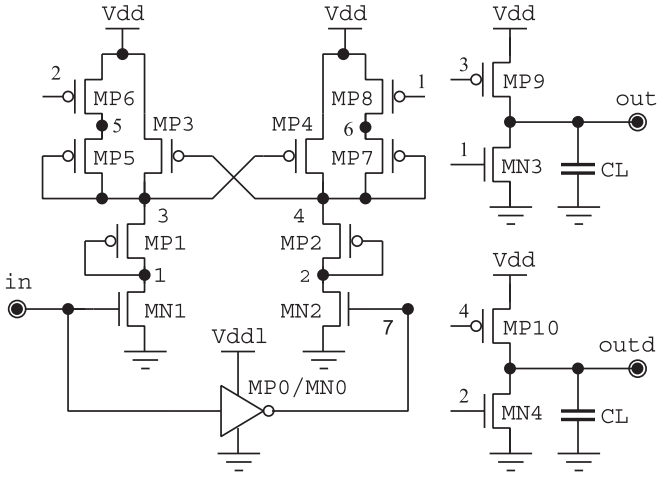

Fig. 1. The circuit diagram for level up shifter of reference [6], *SC1*.

its pull–up section. Unfortunately, *SC1* introduces static power penalty, owing to the first stage used for converting signals between the two different above–threshold voltage domains. To address this problem, we propose a simple structure designed with four inverters and two additional NMOS transistors, as shown in Fig. 2. This proposed shifting circuit, *SC2*, does not use diode–connected PMOS transistors which reduces power consumption due to the alternate turn on of NMOS transistors. The output swing at nodes `out` and `outd` is controlled by inverters `MP3/MN3` and `MP4/MN4`, respectively.

When `in` goes high (and `ind` goes low), node `2` switches to ground level and node `1` pulls up due to inverter `MP2/MN2`, thus node `out` is pulled up to `Vdd` using inverter `MP4/MN4`, and node `outd` is pulled down helped by inverter `MP3/MN3`. On the other hand, when `in` goes low (`ind` goes high), nodes `out` and `outd` are set to low state and high state, respectively. The feedback between the output of inverter `MP2/MN2` and the input of inverter `MP1/MN1` forces the output states to switch on the rising edge of node `in`. The operation of *SC2* is only limited by threshold voltage of the input transistors `MN5` and `MN6`, and the output capacitive load `CL`. Large values of `CL` increase delay and consume high power.

Table 1 presents the active area occupied for each level shifter. The channel length for all transistors is 65 nm. The active area required for level up shifters *SC1*, and *SC2* are 19.82 μm^2, and 4.42 μm^2, respectively, a 77.6% saving in the favor of proposed design. This transistor sizing is optimized considering minimal EDP as figure of merit.

Fig. 3 provides the prelayout simulation results for both of the level shifters. It shows delays for *SC1* and *SC2* considering a square signal

Table 1
Channel widths for transistors for *SC1*, and *SC2*.

Transistor(s)	Type	Width (μm)
SC1 (Active area = 19.82 μm^2)		
`MP1` and `MP2`	P	7 × 10.0
`MP3` and `MP4`	P	1 × 4.0
`MP5`, `MP6`, `MP7`, and `MP8`	P	1 × 0.25
`MP9` and `MP10`	P	1 × 10.0
`MN1` and `MN2`	N	6 × 10.0
`MN3` and `MN4`	N	1 × 8.0
SC2 (Active area = 4.42 μm^2)		
`MP1` and `MP2`	P	1 × 0.8
`MP3` and `MP4`	P	1 × 10.0
`MN1` and `MN2`	N	1 × 0.25
`MN3` and `MN4`	N	1 × 8.0
`MN5` and `MN6`	N	2 × 7.5

Vthn = 0.28 V, and Vthp = −0.2 V

of 0.5 V at `in` and a capacitive load of 450 fF with both circuits. Note the output full swing in these two designs. Maximum value of the load capacitor for *SC2* can be 50% greater than maximum used for *SC1*. Compared with delay of *SC1*, delay in *SC2* decreases by about 50%. An output buffer is connected as a load for each topology with a PMOS/NMOS width ratio of 80/20. A cascade of five identical buffers are used to apply the input signal in both *SC1* and *SC2*. Furthermore, a 25 fF stray capacitance is connected to the input of each buffer. With `CL` of 450 fF and the running frequency of 500 MHz *SC2* achieves 54% better EDP

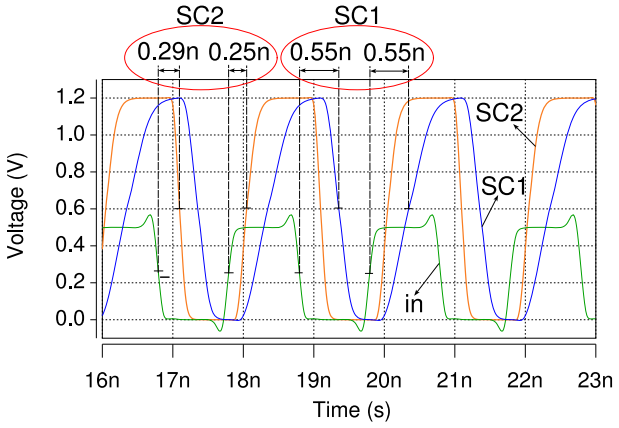

Fig. 3. Pre–layout simulation waveforms for *SC1* and *SC2*. A 450 fF load capacitance is attached to the output nodes.

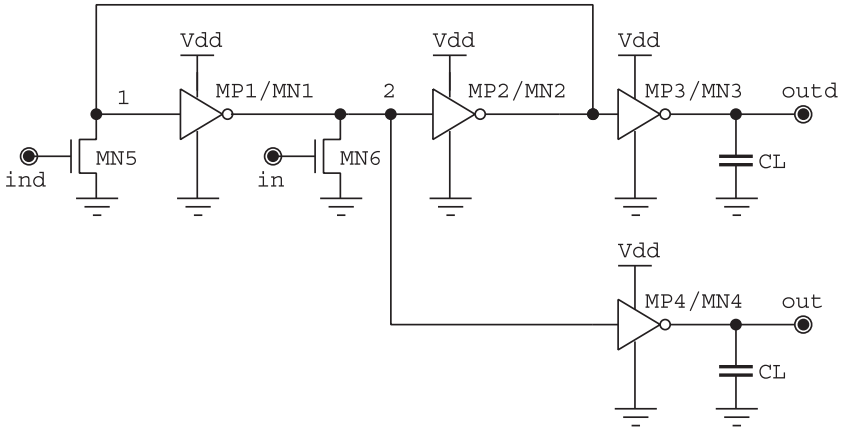

Fig. 2. Schematic for the proposed level up shifter, *SC2*.